A Low-Power Acoustic Periodicity Detector Chip for Voice and Engine Detection

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Introduction
The detection of voices or the rumble of engines is a desirable function in many different devices from toys to smart homes to military applications. Typical approaches involving frequency-domain computation are quite computationally intensive and require a significant power and computational budget. In an effort to construct a very low-power detector capable of acting as a wake-up signal for other systems, we have designed a simple, low-power (1.5uW) analog VLSI circuit that detects periodicity in the time-domain envelope of the acoustic signal.

The circuit takes the input through a peak detector and generates a spike at the onset of a peak. The inter-spike intervals are then converted to a voltage. That voltage is then sampled and stored to be compared with the new sampled voltage. A valid interval that matches (as decided by the interval comparator stage) is called a hit. The circuit can count up to five consecutive hits.

Circuit for Generating Timing Signals
On the negative edge of spike, three independent ramps are triggered with different slopes. As each ramp crosses the threshold of an inverter, a pulse is generated. The first ramp starts the sampling process by pulling the sample pulse low. The second ramp pulls turn off sample high, turning off the sampling pulse. The third ramp turns on the reset pulse. The guard interval can be adjusted to ensure that both the sampling process and the interval comparison have ended before the onset of the reset pulse.

Interval Limiter
The interval limiter defines an acceptance zone defined in terms of voltages $V_L$ and $V_H$. If the stored interval $V_{n-1}$ satisfies the inequality $V_L < V_{n-1} < V_H$, then the two current mirrors will ensure that the two output transistors, M1 and M2, are on pulling the output of the circuit low indicating a valid interval. If the inequality is not satisfied, one of the two output transistors will be off, the output will be pulled up high indicating an invalid interval.

Interval Comparator
The interval comparator decides whether the two “inter-spike intervals”, $V_n$ and $V_{n+1}$, match. $V_n$ sets a current $I_n$ in the differential pair which is split into $I_1$ and $I_2$. $V_{n+1}$ sets $I_{n+1}$ such that $I_n < 1/2$. When the two inputs match, both $I_n$ and $I_1$ are strong enough to hold $V_n$ and $V_{n+1}$ low turning off M1 and M2, and the output is high indicating matched intervals. When the inputs do not match, one of the two output transistors, M1 and M2, is turned on pulling the output low indicating non-matching intervals.

Chip Testing Results
A valid interval together with matching intervals is defined as a hit. Our chip can count up to five consecutive hits.

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