

RESEARCH BRIEF

IMPROVING COMPUTER CHIP HEAT DISTRIBUTION

The challenge

Technology continues to scale down. With the ever increasing density and operating frequency of today's nanometer integrated circuits, the operating temperature of a typical computer chip can easily rise up to 150 degrees Celsius (302 degrees Fahrenheit). This leads to highly unreliable and error-prone chip behavior, degraded performance, and sometimes even breakdowns. In addition, variations and randomness induced by the manufacturing process as well as the unpredictable computing workload scheduled on the chip make the situation more difficult. All these will cause an uneven and hard-to-predict heat distribution on the chip.

As a first step in addressing thermal problems, it is essential to be able to accurately estimate the thermal profile of the chip using runtime information. On-chip thermal sensors can be implemented, but the sensors can be affected by noise and various fabrication randomness. It is important to design and place sensors smartly to minimize overhead.

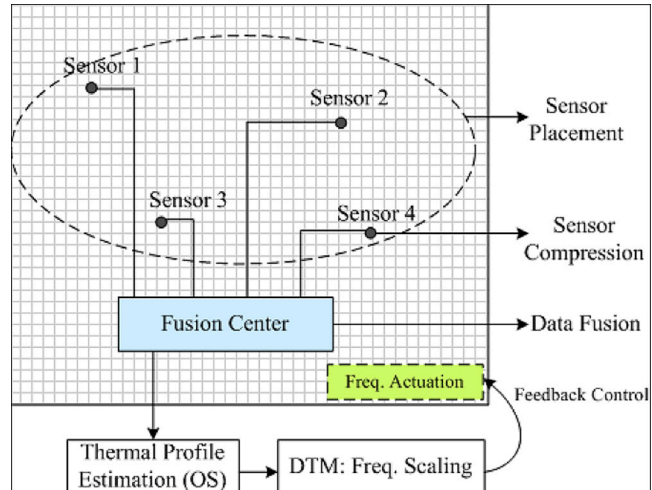
The location and number of such thermal sensors are highly constrained due to area and power considerations. Moreover, sensors at such nanoscale dimensions are also noisy and error prone. The problem remains as how to effectively estimate the temperature for the entire chip given only a few sensors.

The research

Associate Professor Ankur Srivastava and his team have developed a strategy for thermal data mining using on-chip temperature sensors that can provide runtime temperature information. Their goal is to improve the performance and reliability of multicore processors.

Using the Poisson Equation, which governs the relationship between the heat distribution and power dissipation of the chip, Srivastava's team obtains an accurate model for the underlying thermal problem. From there they use statistical strategies to explore the correlations between the power dissipation of different chip modules.

The idea is that, due to these correlations, temperatures at certain sensor locations can be used to obtain thermal



A placement scenario for a reduced number of sensors that would best exploit thermal correlations on a computer chip.

information at other locations as well. Thus, a few thermal sensor readings can be combined with power correlation information to effectively construct the thermal profile for the entire chip. Through experiments, this methodology has demonstrated high accuracy compared to other estimation schemes.

The team also is working on ways to make the sensors more robust to noise and compress them for minimal area and power overhead. In addition, Srivastava is exploring the optimum placement for the reduced number of sensors that would best exploit the thermal correlations; and fusion center design: a way to use hypothesis testing to reconstruct accurate sensor temperatures from the compressed and noise-corrupted sensor readings.

Further research

In 2009 Srivastava and Professor Prakash Narayan were awarded an NSF grant for "Information Theoretic Multi-Core Processor Thermal Profile Estimation" that will extend the thermal management research. The two ISR professors will address new problems in information theory inspired by rate distortion and compressed sensing. The approach has wider applicability to general problems of parameter estimation based on limited sampled and quantized measurements.

Research coming from the new grant should improve the performance and reliability of multicore processors; and introduce new models and problem formulations in information theory and compressed sensing.

Link

View a poster of this research at www.isr.umd.edu/SS2008/2009_posters/Srivastava_chip_fever.pdf

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