

The INE “Word-Serial AER Workshop” at the University of Pennsylvania December 3, 4, and 5, 2005

Application Deadline: Friday, September 16, 2005

Organizers

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Motivation

By transmitting a silicon neuron’s address instead of its spike, N dedicated wires can be replaced with $\log_2(N)$ shared wires. These **address-events**, as they are called, utilize the speed of metal wires, which is wasted when a wire is dedicated to a single neuron. Sharing bandwidth this way enables larger neural networks to be built—and address-events can be rerouted whereas metal wires cannot. But, until now, connectivity could not extend to multichip systems because this decade-old technique did not distinguish one chip from another. The **word-serial** address-event representation (AER) introduced recently by the Boahen lab overcomes this limitation: It appends chip addresses to row and column addresses—all of which are transmitted sequentially—thereby distinguishing one chip’s events from another’s. In addition to being expandable, word-serial is efficient: it cuts the number of address lines in half.

Goals

The primary goal of our workshop is to have participants **leave with a chip design** (*finished* layout) that incorporates a core circuit from their particular research area into a word-serial AER transmitter (and/or receiver) frame. PCs with Tanner Tools fully operational will be provided by the workshop and thus all designs must be compatible with the L-Edit software suite upon arrival.

Preparation

- 1) Applications should take the form of a Mosis MEP proposal: A **three-page** description of the chip, design environment, intended fabrication process, estimated die size, packaging requirements, and plans for testing and characterization. For more information, see <http://www.mosis.org/products/mep/mep-research-proposal.html>.
- 2) Up to 10 participants will be notified of acceptance by **Monday, October 10, 2005**: For U.S. participants, the workshop will cover travel expenses (up to \$500) and hotel expenses (reservations arranged by us). For foreigners, only hotel expenses can be covered.
- 3) Participants must arrive with a completed layout of their neural circuit that satisfies technical (electrical/layout) specifications for interfacing with the word-serial transmitter/receiver circuitry spelled out in: http://www.neuroengineering.upenn.edu/boahen/meth/fs_tools.htm

Workshop

Day 1: *Compile and verify small chip.* In the morning session, starting with a tutorial on ChipGen to kick things off, you will compile a small version of your chip (without pads) and get it to DRC. In the afternoon session, you will get your small chip to LVS and compile a full-size chip (with pads) for overnight DRC and extraction.

Days 2: *Compile and verify full chip.* In the morning session, you will get your full-size chip (extracted overnight) to LVS. In the afternoon session, starting with a tutorial on the transmitter and receiver circuitry to kick things off, you will simulate your small chip—while you continue to run DRC and extraction on the big chip in the background.

Day 3: *Revise, recompile, and reverify.* On this last day, you will go through the design cycle a second time to arrive at your final layout. We finish with a celebratory dinner and everyone heads home.

Funding provided by NSF and CAD tools donated by Tanner EDA, Inc.