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MODELING THE IMPACT OF EMBEDDING PASSIVES ON MANUFACTURING SYSTEM PERFORMANCE

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ABSTRACT

With the miniaturization of electronic products, reducing the size of the printed circuit board that forms the backbone of the product is paramount. Embedding passive components, which otherwise occupy valuable "real estate" atop the printed circuit board, into the printed circuit board substrate itself is one way of achieving this objective. This first part of this paper examines the techniques and advantages of embedding passives.

Embedding passives also affects manufacturing system performance, due to a change in the processing sequence and changes to the processing times at resources. The latter portion of this paper describes a design for production tool for understanding the impact of embedding passives on the performance of a manufacturing system.

KEYWORDS : design for manufacture, design for production, embedded passives, printed circuit boards

INTRODUCTION

In applications such as consumer and industrial electronic products, a printed circuit board (PCB) (or printed wiring board (PWB)) forms the backbone of the device. The PCB substrate supports the discrete components that form part of the circuit along with the wiring requirements for these components. The components may be passive devices (such as resistors and capacitors) or active devices (such

as diodes, integrated circuits, and transistors). These components may be mounted on one side of the substrate or on both sides depending on the circuit's requirements and the size of the board. Usually, the substrate is constructed by laminating copper to one or more surfaces of a sheet of plastic reinforced by paper or glass fiber. Single layer, single sided boards have only one circuit layer. Single layer, double sided boards have two circuit layers, one on each side of the board. Multilayer boards have three or more circuit layers made by bonding (or laminating) layers of patterned, pre-etched, undrilled copper-clad laminate together. Layer interconnections are then made by drilling and plating through holes in the non-conducting plastic.

As circuits become more complicated, they require more discrete passives. In addition, smaller electronic devices require smaller PCBs, which requires shrinking the size of the passive components and developing alternative technologies to accommodate the large numbers need for device functionality. Embedded (or integrated) passive components, which are part of or buried in the PCB substrate and are fabricated along with the substrate [1], may be one way of realizing these goals.

The National Electronics Manufacturing Initiative (NEMI) defines embedded passives as functional elements either buried in or incorporated on the surface of an interconnecting substrate. For more information, see, for example [2, 3, 4, 5, 6, 7].

There are several potential advantages and some shortcomings to embedding passives into the PCB substrate:

1. Increasing the number of embedded components, particularly resistors, decreases the total board area.

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2. Embedding passive components reduces the wiring (the tracks on the outer layer of the board) needed for connecting the components to one another, though the wiring density requirements increase. It may be possible to fabricate more boards from the same panel. Additionally, it may be possible to embed capacitors directly under the active component they support, thereby reducing the number of layers and interconnecting vias.

3. The area processes used to fabricate embedded passives tend to make all components bad when they fail, unlike assembly, which can be corrected for a failed component. It is therefore advantageous to include the passive layers near the bottom of the substrate (and during the initial portion of the processing sequence) so that the low yield steps are included early and defective boards are discarded or reworked early. Due to an increase in the board complexity, the yield could decrease. On the whole, embedding passive components could reduce engineering and manufacturing flexibility.

4. Embedding passive components reduces assembly time and costs, could increase assembly level yield, and may reduce the rework needed in assembly.

5. Using embedded passives increases active circuit density, improves electrical performance, and improves reliability. Electrical connections are shorter and electrical properties of each device are improved through additional termination and filtering opportunities. Product quality improves due to fewer incorrectly soldered passive devices on the PCB, which increases reliability.

6. The increase in cost due to embedding passive components remains constant up to a certain number of passive components (since forming one is as easy as forming many in an area process). Thus, embedded passives become cost effective when a large number of components in a circuit can be fabricated in a single run. Cost savings are associated with eliminating discrete resistors, rework reduction, board densification, and more streamlined assembly processes. The cost of the device may be further reduced by introducing manufacturing automation in making PCBs with embedded passives.

Thus, though embedding passives requires additional processing steps, removing discrete passive components can result in streamlined assembly, less rework and greater overall circuit design flexibility. Specific predictions of the economic and technological advantages of embedding passive components are presented by NEMI [8] in their annual roadmaps. The roadmaps also contain projections of a continuous increase in requirements for embeddeds and associated technologies.

When evaluating the costs and benefits of embedding passives, a product development team must consider the issues listed above and site-specific factors such as the impact on manufacturing system performance. Changing the PCB design will likely change its processing sequence and affect manufacturing cycle time, resource utilization, and other measures. Reducing the manufacturing cycle time has several benefits that impact profitability, including reduced inventory, improved product quality through early detection of process defects, faster response to customer orders, and increased flexibility [9]. This paper presents a model for helping a product development team understand how embedding passives affects manufacturing system performance.

The remainder of this paper describes the models for estimating processing times for the steps required to produce PCBs with embedded passives. After discussing the design for production approach used, the paper presents an example that illustrates the impact of embedding passives on manufacturing system performance.

ESTIMATING PROCESSING TIMES FOR PCBs WITH EMBEDDED PASSIVES

This section presents models that, given the PCB design parameters, estimate the processing times for each step where the design parameters affect the processing time. The models are used by the process planning module of the DFP tool described in the next section.

Design

There are different techniques for embedding passive components into the PCB substrate. One of the technologies widely employed is known as Ohmega-Ply[©1]. The following explanation of the technology is described by Signer [10] and the Ohmega-Ply[©] technical manual [11].

Ohmega-Ply[©] is compatible with existing printed board processing and the material system has few dimensional constraints. The material system is copper foil, to one side of which a metal alloy film is applied. This is then laminated to a polymer substrate such that the alloy film contacts the substrate. The materials come with resistive sheet values of different ohm-per-square and cover a large number of applications.

During processing to create the resistor, the etching is controlled in different passes so that, in certain portions, both the foil and the resistive metal alloy film are etched, and in other areas the foil is etched but the resistive film

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[1]Ohmega-Ply is a registered trademark of Ohmega Technologies, Culver City, California

remains. Two foil areas connected by only the resistive material form a resistor connecting the two areas.

Let R be the resistance of a buried resistor

$$R = \rho_s \, N, \qquad (1)$$

where

$$
\begin{aligned}
\rho_s &= \text{sheet resistance of material, } \Omega/\text{square,} \\
N &= \text{number of squares,} \\
&= \frac{L}{W} \\
L &= \text{length of resistor element, and} \\
W &= \text{width of resistor element.}
\end{aligned}
$$

Figure 1 shows these parameters. The shaded squares correspond to the number of squares in the embedded resistor. The resistance of the resistor shown in the figure is $5\rho_s$ Ω.
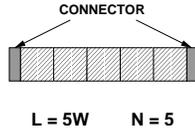

CONNECTOR

L = 5W   N = 5

Figure 1: **Resistance of an embedded resistor**

An advantage of this system is that all manufactured units fall within acceptable tolerance limits of the PCB production processes employed. The limitations of the technique are that since it is a polymer based technology, the units cannot be used in high temperature applications and the initial resistivity tolerances are higher since the parameter depends on the material sheet resistance tolerance and element dimensions. Figure 2 shows differentially defined layers forming separate patterns of conductors (copper members) and resistors formed using subtractive PWB print and etch techniques. Figure 3 depicts the cross-section of a PCB with an embedded resistor and capacitor.

A significant design change for a PCB with embedded passives is a likely change in the resulting number of layers. The number of layers in the PCB greatly influences the total processing time.

Sandborn et al. [6] present a model to find the number of layers needed for a PCB with embedded passives. This research modifies the model presented there. Let us define
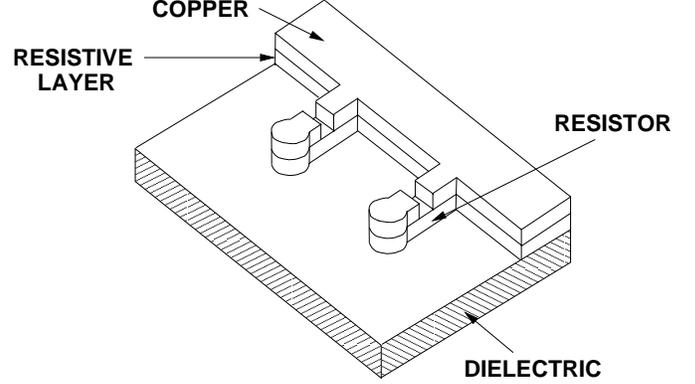

COPPER

RESISTIVE LAYER

RESISTOR

DIELECTRIC

Figure 2: **Embedded Resistor [12]**

the following notation:

$$
\begin{aligned}
N_l^c &= \text{number of layers for conventional board} \\
&\quad \text{(no embedded passives),} \\
U &= \text{Usage Limit} \\
&\quad \text{(Fraction of wiring that is used to route} \\
&\quad \text{the application),} \\
N_{IO}^c &= \text{total number of IO in the conventional} \\
&\quad \text{implementation,} \\
N_R &= \text{number of embedded resistors,} \\
N_{BC} &= \text{number of embedded bypass capacitors,} \\
A_{R_i} &= \text{area occupied by the embedded resistor } i, \\
A^c &= \text{conventional board area,} \\
W_r &= \text{ratio of wiring needed for new board to that of} \\
&\quad \text{a conventional one.}
\end{aligned}
$$

Given these parameters for a PCB, we can determine the number of layers N_l^n for the new board (with embedded passives) as follows:

$$f = \frac{N_{IO}^c - 2N_R - 2N_{BC}}{N_{IO}^c} \qquad (2)$$

$$N_l^n = W_r \left[f N_l^c + \frac{\sum_{i=1}^{N_R} A_{R_i}}{A^c U} \right] \qquad (3)$$

U may take a value between 0.1 and 0.9 since the actual area available for wiring is less than the total board area.

The following are the critical design parameters for a PCB (with or without embedded passives):

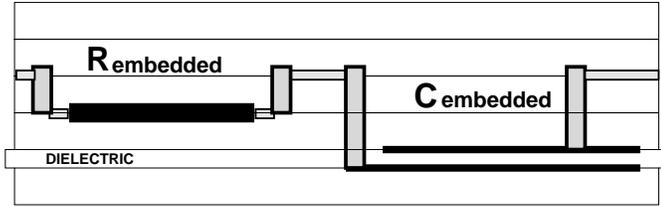1. Board dimensions (length and breadth),

Figure 3: **Cross-section showing embedded passives [8]**

2. Total wiring requirements,

3. Number of layers,

4. Number of embedded resistors,

5. Number of embedded capacitors,

6. The set of active component types and the number of each type,

7. Thickness of the board,

8. Number of discrete resistors, and

9. Number of discrete capacitors.

Some design parameters listed above depend on other design parameters. For example, the size of the board is defined by the number of embedded and discrete passives and total wiring requirements, the total wiring requirements are governed by the number of embedded and discrete passive components in the PCB, and total number of layers in the PCB depends on the size of the board, the number of embedded and discrete resistors and bypass capacitors.

The decision on the number of passives to embed is taken keeping under consideration the total number of passive components on the PCB, the resultant size of the board and the number of layers in the resulting PCB design. The thickness of the board is directly influenced by the number of layers in it. The number of discrete resistors and capacitors to be soldered atop the PCB depends on the total number of passives in the design of the PCB and the quantity to be embedded.

Processing Steps for PCBs

Based on information from the manufacturer and details presented by Coombs [13], manufacturing a printed circuit board involves the following steps (the symbols indicate the notation for the mean processing time for that step):

1. Apply resist to internal layers, t_{RA_l}

2. Generate artwork for internal layers, t_{A_l}

3. Develop-Etch-Strip (DES) for internal layers, t_{DES_l}

4. Test internal layers, t_{T_l}

5. Drill holes for vias, t_{D_l}

6. Desmear layer, t_{DS_l}

7. Plate via holes in layer, t_{P_l}

8. Kitting and Layup, t_{KL}

9. Lamination, t_L

10. Drill holes for pin hole through components, t_D

11. Desmear board, t_{DS}

12. Electrolysis plate for board, t_P

13. Apply resist to board, t_{RA}

14. Artwork/Exposure of board, t_A

15. DES board, t_{DES}

16. Inspect board, t_I

17. Solder level, t_S

18. DES for solder, t_{DES_s}

19. Final routing check for board, t_{RC}

20. Final inspection for board, t_{I_f}

21. Separate boards from panel, t_C

22. Print solder paste (side 1), t_{PS_1}

23. Place discretes on side 1, t_{a_1}

24. Inspect assembly, t_{I_1}

25. Print solder paste (side 2), t_{PS_2}

26. Place discretes on side 2, t_{a_2}

27. Reflow solder connects, t_{I_2}

28. Final assembly, t_{a_f} and

29. System test t_{T_s}.

The above steps are valid for PCBs without embedded passives. A PCB with embedded passives needs two additional steps executed prior to the Kitting and Layup operation. The first step, which we label Embedding 1, has a mean processing time denoted by t_{E_1} and includes the following five tasks:

1. Apply photoresist polymer,

2. Expose polymer to create vias,

3. Cure dielectric polymer,

4. Develop photoresist, and

5. Strip photoresist.

The second step, which we label Embedding 2, has a mean processing time denoted by t_{E_2} and includes the following six tasks:

1. Apply photoresist,

2. Print conductor protection pattern,

3. Electroless plate resistive layer,

4. Etch copper remove excess,

5. Strip photoresist, and

6. Measure values and clean.

Effects of Embedding Passive Components

The process for a PCB with embedded passives is different from the process for a PCB with none. Moreover, each additional embedded passive modifies the processing time of the required steps. The changes also depend on the type of passive component being embedded.

When the manufacturer decides to embed discretes into the PCB substrate or add a new layer to the PCB, the following factors need to be considered while defining the design and processing parameters for the PCB:

1. The overall drill time increases due to the addition of each new layer to the board. The tool wear is also likely to increase due to the increase in board thickness. This requires more tool change (and setup) time for the same panel.

2. When the first passive in embedded, additional steps associated with the embedding process are added to the process plan for the PCB (as stated above).

3. Adding a layer from embedding a passive device increases the time required for the kitting operation, the layup operation, and the lamination operation.

4. Embedding the passive devices imposes restrictions on the assembly sequence of the PCB. Since errors in the layers having embedded passives are not easily rectifiable, it is necessary to complete and test such layers before making assemblies or sub-assemblies with these layers. Thus they influence the overall processing sequence for the PCB.

5. It may be possible to eliminate the surface mounted components or the pin-through hole components on one side of a double sided PCB by embedding passives into the substrate. Eliminating all discretes on one side of the board would result in a tremendous saving in time, since the PCB needs to pass through the assembly process only once.

Each time an additional discrete component is embedded, design and processing modifications occur for the PCB. These changes, though not as dramatic as the ones listed above, nevertheless need to be kept under consideration while analyzing the PCB.

1. Reducing the number of components to be surface or through-hole mounted reduces assembly time for the PCB.

2. Reducing the number of holes to be drilled (corresponding to the passive that has been embedded) lowers the processing times at the drilling and deburring stations.

3. Embedding an additional passive may increase the board area and the time taken for printing the artwork on the board.

4. Embedding a passive component may reduce the surface area of the board meaning more boards can be fabricated from a panel. This in turn means that the setup time per board is reduced for steps that process panels, which now make more boards.

5. Embedding a passive without adding a new layer occupies some of the area of the board, and this area is blocked and cannot be used for wiring (i.e. laying tracks to connect the various components that the PCB supports).

Processing Time Models

The processing times for the PCB at various workstations are most often affected by the area of the PCB, the area of the panel and the number of layers. Based on discussions with experts on manufacturing electronic packages, we identified that nearly all steps mentioned in the earlier subsection are affected by the board area or the number of boards that can be made from one panel, which in turn is determined by the board area (since the panel area is generally constant).

In addition, the number of layers affects many processes, including resist application, artwork, develop-etch-strip, kitting, laminating, and embedding. The time required for drilling depends on the number of holes necessary, which in turn depends on the number of discrete components. The time for the assembly operations to mount these discretes also depends on their number. The processing time for lamination depends on the time taken for the

Table 1: **Product design parameters**

Notation

l_b	length of board
b_b	breadth of board
n_{dR}	number of discrete resistors
n_{dC}	number of discrete capacitors
n_{bC}	number of bypass capacitors
n_{a_i}	number of active components of type i
$\mathcal{A}$	set of active component types
n_{lb}	number of layers for board

Table 2: **Manufacturing parameters**

Notation

d_b	spacing between boards
a_p	area of panel
s_f	feature size of embedded resistor
T_l	layer thickness
T_p	prepreg thickness
θ_c	board material heat transfer coefficient
r_d	drill feed rate
t_c	time to cut board
h_i	number of holes required by a component of type i
t_{d_a}	time for assembly (discrete)
t_{b_a}	time for assembly (bypass)

intermediate prepreg layers to melt. This in turn is a function of the heat coefficient for the prepreg material. Based on literature on PCB manufacture, we analyze the lamination process using the lumped parameter approach for two dimensional heat conduction. The total time needed to separate all boards on a panel depends also on the time taken to separate each board. The processing times for the embedding steps depend upon the number of embedded passives and the number of layers. The design parameters and constants for the product are listed in Table 1 while the manufacturing parameters are listed in Table 2.

The models presented here assume that each layer of the PCB is treated as an individual product until the kitting stage. The layers travel in batches from one workstation to another through the system. Once the layers are laminated together, they travel as part of a panel. Each board also travels as part of a panel from the lamination stage to the separation stage. Such panels travel in batches through the system. Until the stage where the separation of individual boards occurs, the board travels as part of a panel (which may contain more than one board depending on the size of the board).

After the separation stage, the boards travel in batches

through the system. The number of boards in a batch may be less than, equal to, or greater than the number of boards that are separated from one panel. Each discrete resistor and capacitor has two leads. This in turn means that two holes are needed for assembly of a discrete passive on the PCB. Further, the effects of these changes in material movement units are modeled as factors, F_{bp} and F_{pl} explained below.

The following equations are used to calculate intermediate quantities, which are functions of the product design and manufacturing parameters. These are then used in calculating the mean processing times for the various steps.

$$T_b = n_{lb}T_l + (n_{lb} - 1)T_p \tag{4}$$

$$n_h = 2(n_{dR} + n_{dC}) + \sum_{i \in \mathcal{A}} n_{a_i} h_i \tag{5}$$

$$a_b = l_b b_b \tag{6}$$

$$n_{bp} = \frac{a_p}{(a_b + d_b(l_b + b_b))} \tag{7}$$

$$F_{bp} = \frac{1}{n_{bp}} \tag{8}$$

$$F_{pl} = n_{lb}F_{bp} \tag{9}$$

$$A_R = s_f^2 N_R \tag{10}$$

T_b	=	board thickness
n_h	=	number of holes in board
a_b	=	board area
n_{bp}	=	boards per panel
F_{bp}	=	factor: board-panel
F_{pl}	=	factor: panel-layer
n_{lb}	=	N_l^c if the PCB is a conventional board,
	=	N_l^n if it has embedded passives

We model the mean processing times as functions of the design parameters. These processing time models for the various operations are listed in Table 3.

Discussion

The models presented here show that the impact of embedding passives is significant and complex. Thus we can make no general statements about the system-level impact of embedding passives components. A product development team should collect the required data, employ the models presented here (modified as necessary to reflect site-specific issues), and estimate resource utilization and manufacturing cycle time using the DFP approach.

Table 3: **Product processing times**

Operation	Processing Time Relation (in min.)
t_{RA_l}	$0.01 F_{pl} a_p$
t_{A_l}	$4 F_{pl}$
t_{DES_l}	$0.008 F_{pl} a_p$
t_{T_l}	$0.8 F_{pl}$
t_{KL}	$0.4 F_{pl} n l_b$
t_D	$5 + F_{bp} \frac{T_b}{r_d} n_h$
t_L	$10 + F_{bp} \theta_c T_b$
t_{DS}	$2 + 20 F_{bp}$
t_P	$7 + 10 F_{bp}$
t_{RA}	$0.2 F_{bp} a_p$
t_{DES}	$5 + 20 F_{bp}$
t_I	$10 + 20 F_{bp}$
t_{E_1}	$0.8 + 3.8 F_{pl}$
t_{E_2}	$0.5 + 4.2 F_{pl}$
t_S	$0.1 F_{bp} a_p$
t_{DES_s}	$0.2 F_{bp} a_p$
t_{RC}	$5 + 20 F_{bp}$
t_{I_f}	$2 + 2 F_{bp} n_{bp}$
t_C	$2 + F_{bp} t_c$
t_{PS}	$0.05 a_b$
t_a	$\frac{n_{dR} + n d C}{100}$
t_I	$1.2 \frac{n_{dR} + n d C}{100}$
t_{a_f}	$(n_{dR} + n_{dC}) t_{d_a} + n_b C t_{b_a}$
t_{T_S}	10

Figure 4: **Schematic for a DFP Tool**

DESIGN FOR PRODUCTION

For evaluating the impact of embedding passives on manufacturing system performance, this paper adopts the design for production (DFP) approach introduced by Herrmann and Chincholkar [9, 14, 15, 16]. Manufacturing cycle time (also known as throughput time or flow time) is the total time spent by each part of a product and consequently the product itself in the manufacturing system. It comprises the actual processing time for the product at the various workstations that it must visit along with the idle time that it spends waiting to be processed. The latter time often dominates the total time and arises from queuing at heavily utilized workstations. The term design for production describes methods that evaluate a product design by comparing its manufacturing requirements to available capacity and estimating manufacturing cycle time. These methods require information about a product's design, process plan, and production quantity along with information about the manufacturing system that will manufacture the product.

Other researchers have used various names to describe DFP approaches, including design for existing environment [17], design for time-to-market [18, 19], design for localization [20], design for speed [21], design for schedulability [22], and design for manufacturing system perfor-
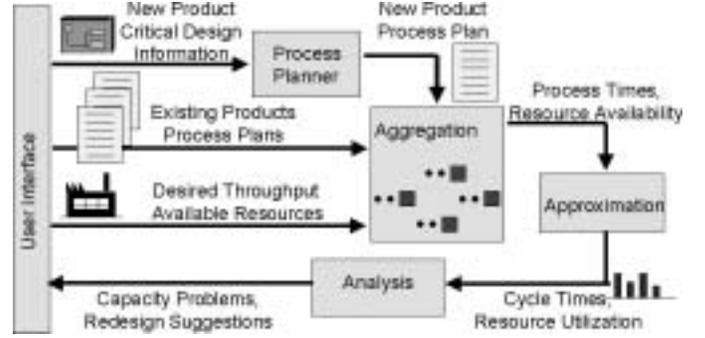
mance [23]. Some of these researchers have reported case studies in which product designs were modified to improve production. Most of the work has been in three areas of DFP: design guidelines, capacity analysis, and estimating manufacturing cycle times. See Herrmann and Chincholkar [15] for a more detailed review of DFP approaches and the relative merits of using fixed lead times, mathematical models, discrete-event simulation, and other techniques.

DFP will become more important as product variety increases and product life cycles decrease. Factories will then be faced with an explosion of varying manufacturing cycle times because of the increased product variety, and historical manufacturing cycle times will not be accurate enough for estimating the times for a new product to be manufactured in the future, when the product mix is different. Additionally, since production lines usually outlive individual products, it is prudent to design new products that can be manufactured quickly using existing equipment.

As explained above, the Design for Production approach models the relationship between the product and the manufacturing system processing the set of products. In order to be able do this analysis, adequate knowledge of the product and processing system parameters is essential. This section presents the various models integral to the DFP approach, which we have implemented as a DFP tool.

As seen from the schematic in Figure 4, a DFP tool consists of an user interface along with a process planning module, an aggregation module, an approximation algorithm, and an analysis module. The user interface allows the user to input the product design and the key characteristics for the products being processed in the manufacturing system. The process planning module uses the product design information to find the processing times for the product and its components at the various resources that form a part of the product processing sequence.

For representing the manufacturing system, the DFP tool uses a queuing network model to estimate the average manufacturing cycle time of products. The approximation

aggregates the products and calculates the average manufacturing cycle time at each workstation. This model uses previously described approximations [24, 25].

This manufacturing system model assumes that the manufacturing system will complete a large number of work orders (jobs) of the new product. No job visits a workstation more than once. This model assumes that the product mix and the resource availability do not change significantly over a long time horizon. Of course, it may be possible to divide the time horizon into two or more periods where the system reaches steady state. In this case, this model can be used for each time period. Alternatively, one can neglect the aspects of the system that are evolving and use the steady state model to approximate the system.

For more information on queuing network models, see Papadopoulos et al. [26] and Buzacott and Shanthikumar [27], who present queuing network models for manufacturing systems. Connors et al. [28] modeled semiconductor wafer fabrication facilities using a sophisticated queuing network model to analyze these facilities quickly by avoiding the effort and time needed to create and run simulation models. (These models are similar to the ones used here.) They present numerical results that show how the queuing network model yields similar results to those that a simulation model yields. Koo et al. [25] describe software that integrates a capacity planning model and queuing network approximations. They report that the approximations are reasonable when variability is moderate.

The aggregation module calculates, for each product, the mean processing time of each job at each workstation. It also calculates, for each workstation, the average processing time, weighted by each product's arrival rate. Finally, it modifies the aggregate processing times by adjusting for the resource availability.

The queuing network approximations used in the tool, all based on previously described models, offer some advantages and also have limitations. Compared to simulation models or more sophisticated queuing network analysis techniques, these approximations are less accurate, especially for very complex systems, and cannot provide the same range of performance measures. However, they require less data and less computational effort than the simulation models and other analysis techniques. Therefore, they are more appropriate for situations where a decision-maker needs to compare many scenarios quickly.

To describe the predicted performance of each workstation in the manufacturing system, the DFP tool estimates the resource utilization and the manufacturing cycle time at the resource. Resource utilization defines the percentage of the total time that the workstation is busy processing parts. This in turn influences the time that a part arriving at the workstation has to wait before it can begin processing. The utilization is a function of the arrival rate for the product and the processing time for the product at the workstation.

For a system processing multiple products, the arrival rates and processing times need to be aggregated over the product set in order to find this utilization.

$$u = \frac{t^\star}{n} \sum_{i \in V} x_i \qquad (11)$$

where

u = the average resource utilization,
$t^\star$ = modified aggregate process time at the workstation,
n = the number of resources in the workstation,
x_i = release rate of product i (jobs per hour), and
V = set of products that visit the workstation.

The manufacturing cycle time for each workstation contributes to the total manufacturing cycle time for the product and is, hence, another important performance estimation parameter for the processing system. As in the case of the resource utilization, for a system processing multiple products, it is necessary to average the resource cycle time over the set of products visiting the resource. The tool uses the following manufacturing cycle time approximation [24]:

$$CT^\star = \frac{1}{2}(c^a + c^\star) \frac{u^{(\sqrt{2n+2}-1)}}{n(1-u)} t^\star + t^\star \qquad (12)$$

where

$CT^\star$ = average manufacturing cycle time time at the resource,
c^a = SCV of interarrival times at the resource, and
$c^\star$ = SCV of the modified aggregate process time.

The squared coefficient of variation (SCV) of a random variable equals its variance divided by the square of its mean. The SCV is a measure of the variability of the random variable. This model incorporates the variabilities associated with the interarrival and processing times for a product at various workstations. The manufacturing cycle time for a product is the sum of the average manufacturing cycle times for the workstations that constitute the product's processing sequence. This is true for all the products in the product set being processed in the manufacturing system. Thus,

$$CT = \sum_{j \in R} CT_j^\star \qquad (13)$$

8

where

$$CT = \text{the average manufacturing cycle time of jobs of the product,}$$

$$R = \text{the set of workstations that the product must visit, and}$$

$$CT_j^\star = \text{average manufacturing cycle time at workstation } j.$$

For detailed explanation of the mathematical model and calculations, please refer to Herrmann and Chincholkar [14, 16].

EXAMPLE

This section presents an example of using the DFP approach to illustrate impact of embedding passives on manufacturing system performance. The information about the product and the system is based on experiences and information with electronic systems manufacturers. The examples use data that collaborators were able to provide and other synthetic data that was created as part of this research effort. Key characteristics of the example are given below. More details are available from the authors.

Manufacturing System

The manufacturing facility for the product is a PCB fabrication and assembly shop having various types of batch processes, individual part processes, manual inspection, and automated inspection stations. The material handling between workstations, which is automated in the form of conveyor belts, does not contribute significantly to the manufacturing cycle time.

Products

The printed circuit board under consideration is a multilayer board with surface mount components and pin through hole mounted components on both sides of the board. The manufacturer currently makes one type of PCB, called CPU_board, used in a mainframe. The board serves as the central processing unit for the AS900 machine. Due to associated advantages such as reduced costs, improved electrical performance, lower manufacturing and assembly defects, and a heavy utilization of present resources, the manufacturer has opted to embed a portion of the passive devices that are currently assembled using either surface mount or pin through hole technology. The remaining passive devices and the active ones continue to be assembled similarly. Though the company wishes to change the product in this fashion, it needs to continue producing the older product in order to satisfy the requirements of current users, till such time as a total shift to the new product is made.

Table 4: **PCB Design Features**

Design Parameter	Value
Length of board	18 inches
Breadth of board	12 inches
Discrete Resistors	627
Discrete Capacitors	54
Bypass Capacitors	53
Network parts	71
Diodes	53
Zeners	17
Transistors	64
Inductors	28
Transformers	12
ICs	108
Number of Layers	12
Number of Sides	2

Therefore, in the new scenario, the facility will make two products, called CPU_board and CPU_board_new, which contains the embedded passive components. The facility does not manufacture any other product. (It needs to be emphasized, however, that any other products that the facility manufactures can be easily incorporated in the DFP approach in a similar manner.)

The throughput is currently 4.5 boards per hour. The factory intends to reduce the throughput of CPU_board to 3 boards per hour while producing CPU_board_new at a rate of 1.5 boards per hour.

The circuit for the CPU that currently defines CPU_board has the design characteristics detailed in Table 4. The boards are cut from panels 24 inches long and 18 inches wide. Spacing between boards on a panel is 0.15 inches while the length and breadth of the discrete components are 0.04 and 0.02 inches respectively. The active devices as well as the discrete passives components are pin through hole mounted on both sides of the PCB. Of the non-passive devices in the product, the diodes, zeners, and inductors require two holes, the transistors and transformers require three holes while the network parts and ICs require 50 holes.

Each embedded passive has a maximum feature size of 0.015 inches and the PCB has maximum 6361 IOs, with a wiring ratio of 1.1. For detailed explanations of various terms, please refer to Sandborn et al. [6]. The design changes arising out of embedding passives present an option to change the size of the board. This example, however, maintains the same size for the board while calculating the number of layers for CPU_board_new.

Table 5: **Resource utilizations**

Percent embedded	10%	90%
Artwork inner layers	0.94	0.86
Apply Resist inner layers	0.93	0.85
DES inner layers	0.88	0.81

Results

As more passives are embedded in CPU_board_new, the number of layers in the multilayer PCB changes. In conjunction, the processing times for the PCB at the various workstations in the manufacturing system change. This in turn changes the average manufacturing cycle time at each workstation in the product's processing sequence. The overall result of these modifications is that the manufacturing cycle time for the new product is different from that of the existing product, CPU_board.

Figure 5 shows a plot of the manufacturing cycle time for the two products as the percentage of embedded passives increases from 0% to 90%. The case with 0% embedded passives is the current situation of the existing product CPU_board. The case with 90% embedded means that 660 of the 734 discrete resistors, discrete capacitors, and bypass capacitors are replaced with embedded passives.

As the percentage of embedded components increases, the total processing time decreases from 392.77 min. to 379.40 min. when 90% passives were embedded, a decrease of 3.5%. The resource utilization for the three most utilized workstations decreases, as shown in Table 5.

The decreased congestion reduces the manufacturing cycle times for the two products. For CPU_board with all discrete passive components, the manufacturing cycle time is 2659 min. Adding the new product significantly changes the manufacturing cycle time. Increasing the percentage of embedded components from 10% to 90% reduces the manufacturing cycle time of the new product by 15.4% and reduces the manufacturing cycle time of the old product by 14.95%.

SUMMARY AND CONCLUSIONS

This paper described a model for evaluating how embedding passives into a PCB affects not only the processing times at each step in the manufacturing process but also the overall manufacturing system behavior. The product processing time models are functions of the product design parameters. The processing times change as the number of embedded passives changes. Values of certain other PCB design parameters are also affected by the number of embedded passives and these also affect the processing times at various processing stations.

It is important that the product development team understand that their design decisions affect the manufactur-
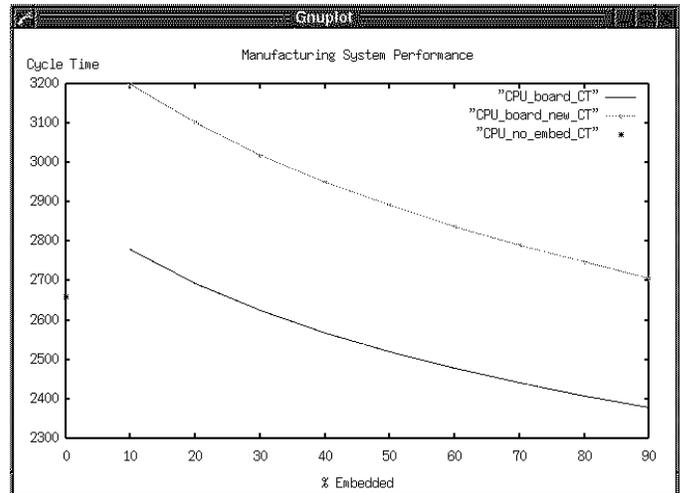

Figure 5: **Manufacturing cycle time with increasing percentage of embeddeds**

ing system performance. Having this feedback early in the design process avoids rework loops needed to solve problems of manufacturing capacity or cycle time.

The results shown here illustrate how the model works and give some ideas of the measures that need to be considered. A product development team should apply the model to the specific system that they will use and should incorporate its results with other information about cost, performance, reliability, and desirability of embedding passives.

Though this paper concentrated on embedding passive components in PCBs, the DFP approach described here is equally valid for any product development process. The details of the model must be varied to reflect the specific situation.

Additional work needs to be done to develop models that incorporate process yield and process drift, which affect system performance, and inventory management and supply chain performance measures, which have important economic impacts.

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