

A CMOS image sensor for low light applications

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Abstract— We describe and analyze a novel CMOS pixel for high speed, low light imaging applications. The new pixel achieves lower dark current and noise and increased gain in comparison with conventional three-transistor, one-photodiode active pixel sensors without sacrificing speed and scalability to large arrays. It accomplishes this by biasing the photodiode of each pixel near zero volts and by separating the photodiode from the floating diffusion integration node. An image sensor with a 256×256 array of these pixels was designed for a commercially available $0.18 \mu\text{m}$ CMOS technology. The pixel size is $5 \mu\text{m} \times 5 \mu\text{m}$ with a fill factor of 31%. The chip area is $3000 \mu\text{m} \times 3000 \mu\text{m}$. 1.8 V and 3.3 V power supplies are used for logic and sensor array, respectively. Differential output and chip level correlated-double sampling are used to suppress fixed pattern noise. Transmission gates with dummy transistors are incorporated into the readout chain to reduce both clock feedthrough and charge injection.

I. INTRODUCTION

The main challenges for CMOS imagers in industrial and scientific applications are their relatively large dark current and random noise, especially at low light. To increase both signal to noise ratio (SNR) and dynamic range (DR) of a CMOS image sensor, prior efforts focused on reduction of reset noise, the dominant temporal noise component of an active pixel sensor (APS), with significant improvement of performance [1]–[3]. Reduction of dark current mainly relies on specialized CMOS imaging processes. Though dark currents less than $0.5 nA/cm^2$ have been reported [4], the spatial distribution was non-uniform and not well-behaved. Pain et al. [5] suggest that dark current may set the ultimate noise limit in CMOS imagers.

Dark current of a CMOS APS pixel is mainly generated as leakage current from the reverse biased photodiode and parasitic junctions. Previous work has shown that dark current increases significantly with increasing reverse bias voltage across the photodiode [6], [7]. Several techniques have been proposed for reducing dark current induced temporal and spatial noise. In [8], a shielded dummy phototransistor was added to compensate dark current of the phototransistor in neighboring pixels. Since the bias conditions for the dummy pixel and neighboring pixels differ, dark current can not be sufficiently removed. The extra dummy pixel also degrades the imager's resolution. Wu et al. proposed a "pseudo-active-pixel-sensor" structure, where each pixel includes only one switch transistor and one photodiode [9], like the passive pixel sensor first introduced by Weckler [10]. They demonstrated that the ratio of photo current to dark current increased by nearly 40dB when the reverse bias voltage was reduced from

3 V to near 0 V. However, since photocurrent is integrated at the column level for each selected row, the frame rate is reduced by a factor of N_{row} , the number of rows, compared to that of a conventional APS given the same integration time. In addition, the scalability of the pixel array is limited because all unselected pixels in each column contribute leakage current to the column-level integration capacitor as well.

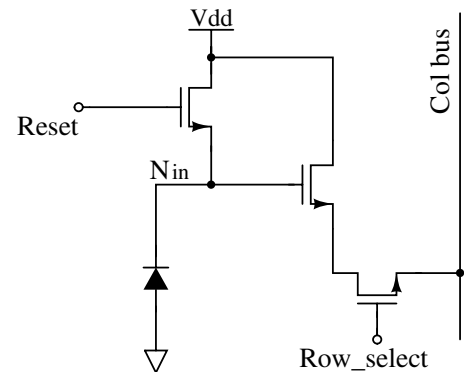


Fig. 1. A conventional three transistor one photodiode pixel.

In this paper, a new CMOS image sensor structure is proposed to achieve low dark current and low noise by biasing all photodiodes near zero volts. One additional transistor is added to a conventional APS pixel, and photocurrent is integrated in the pixel. Thus, it enables low dark current, low noise, and good linearity while retaining the speed and scalability of a conventional APS. Column level differential sampling and chip level correlated double sampling (CDS) are performed to eliminate fixed pattern noise (FPN) due to threshold mismatches of transistors along the readout chain.

The rest of this paper is organized as follows: section II briefly analyzes dark current related artifacts; section III discusses the design and performance of the proposed pixel, column and chip level readout; section IV shows simulation results to demonstrate the feasibility of the proposed structure; and section V summarizes this work.

II. ARTIFACTS INTRODUCED BY DARK CURRENT

The schematic of a conventional three transistor one photodiode APS is shown in Figure 1. During the integration period, the nplus/psub photodiode is usually reverse biased and the bias voltage decreases at a rate of $(I_{ph} + I_{dk}) \times t_{in}/C_{ph}$, where I_{ph} is the photocurrent, I_{dk} is the dark current, t_{in} is the integration time, and C_{ph} is the total capacitance at the integration node N_{in} . An artifact introduced by I_{dk} is

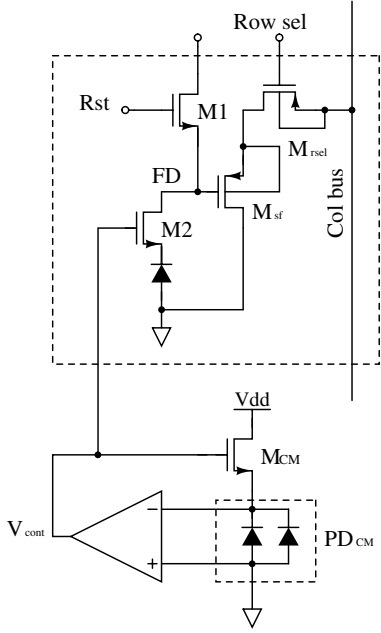


Fig. 2. Low dark current pixel along with chip-level circuits for generating the common gate voltage for the entire pixel array.

the reduction of signal dynamic range. The temporal noise is increased due to shot noise of the dark current, which has a power spectral density of qI_{dk} . In addition, dark current introduces spatial noise due to different reverse-bias voltages seen by photodiodes in different pixels. Another artifact resulting from dark current is nonlinearity since the dark current varies with bias voltage across the photodiode. The linearity is further degraded since both I_{ph} and C_{ph} change with the reverse bias voltage across the photodiode as well. Dark current I_{dk} mainly arises from the surface and bulk leakage current of the reverse biased nplus/psub diffusion area of the photodiode. By biasing the photodiode near zero volts, all artifacts discussed above can be significantly improved.

III. DESIGN AND OPERATION

A. Pixel circuit and operation

Figure 2 shows the schematic of a low-dark-current pixel along with the chip level feedback amplifier that generates the gate voltage for in-pixel common gate transistor $M2$. Similar pixel structures were previously reported. $M2$ is used as a shutter switch in [11], so photocurrent integration occurs at the same time in all pixels. Gonzalez et al. [12] used $M2$ as a transfer gate, similar to the one used in a photogate pixel, so that the reset signal can be sampled before the photovoltage in order to perform a true CDS. Kyomasu used $M2$ as a transfer gate during integration to achieve high conversion gain and good linearity, with the gate voltage of $M2$ generated off-chip. Kyomasu's pixel comprises more than seven transistors and occupies an area of $35\mu m \times 240\mu m$ [13].

While the proposed pixel can be operated as mentioned in [11]–[13], the intention of this work is to bias the photodiode near 0 V in order to significantly reduce dark current and improve related artifacts. To achieve a reasonable pixel size

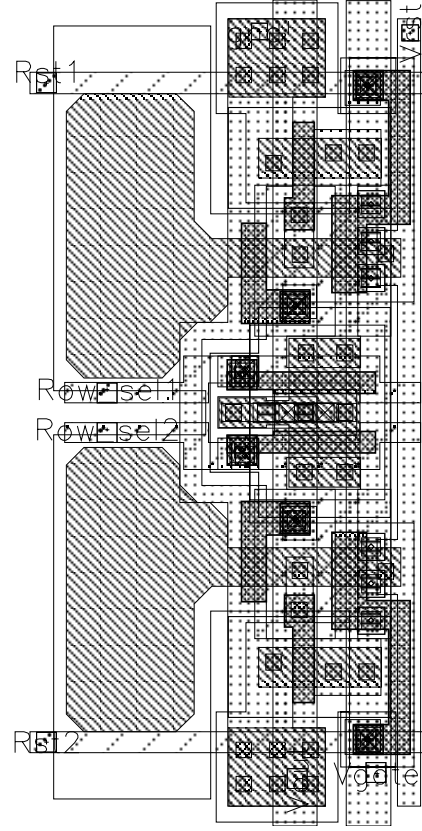


Fig. 3. The layout of two neighboring pixels in one column.

and fill factor, a separate photodiode PD_{CM} is used to generate a global bias voltage V_{cont} for the gate of $M2$. The positive terminal of PD_{CM} is connected to both ground and the positive input of the feedback amplifier. The negative terminal of PD_{CM} is connected to the source of common gate transistor M_{CM} and the negative input of the feedback amplifier. The feedback loop is closed through M_{CM} by connecting the feedback amplifier's output to the gate of M_{CM} . The drain of M_{CM} is directly connected to a 3.3V power supply. The feedback amplifier has a single-stage folded-cascode structure with p-type input transistors in order to operate at a common mode input voltage near 0V. It has output swing from 0.3V to 2.5V, gain of 740 with common mode input as low as 0 V, and unity gain bandwidth of 440MHz.

The gate source voltage V_{gs_CM} of transistor M_{CM} is determined by its drain current I_{ds_CM} . Since I_{ds_CM} is normally on the order of pA or less, M_{CM} operates in the saturated subthreshold region. Therefore, its drain current can be expressed as: $I_{ds_CM} = I_0 \times (W/L) \times \exp(\kappa V_{gs_CM}/V_T)$, where I_0 is the characteristic current, W/L is the geometry factor, κ is the subthreshold slope factor, and V_T is the thermal voltage. V_{gs_CM} is equal to $V_{cont} - V_{s_CM} = -(A+1)V_{s_CM}$, where A is the gain of the feedback amplifier. Thus, the source voltage of M_{CM} is given by

$$V_{s_CM} = \frac{\ln(\frac{I_{ds_CM}}{I_0(W/L)})V_T}{-\kappa(A+1)} \quad (1)$$

Assuming $I_{ds_CM} = 1pA$, $I_0 = 9.5aA$, $W/L = 1.5$,

$\kappa = 2/3$, and $V_T = 26mV$, V_{s_CM} is about $-0.59mV$ and V_{cont} , the output of feedback amplifier, is approximately equal to $435mV$. At this output level, the amplifier gain A actually drops to around 220. However, V_{cont} remains approximately the same given that $V_{cont} = -AV_{s_CM}$, where V_{s_CM} is around $-2mV$.

If an in-pixel photodiode has a photocurrent greater than that of PD_{CM} , this photodiode will be forward biased because of the greater V_{gs} of $M2$ in the same pixel. The photocurrent will thus be partially cancelled by current flowing from ground to the source of $M2$. In order to reduce the likelihood that the in-pixel photodiodes might become forward biased, PD_{CM} is designed to have twice the area of an in-pixel photodiode. PD_{CM} can also be implemented by several photodiodes distributed around the pixel array in order to faithfully represent the background illumination.

Since V_{cont} is a constant voltage for a given background illumination, the voltage across an in-pixel photodiode V_{pd} will also be slightly influenced by the the voltage V_{FD} at the floating diffusion node (FD). As V_{FD} decreases to $3V_T$ from its reset level, the drain current of $M2$ can be expressed as $I_{ds_M2} = I_0 \times (W/L) \times \exp(\kappa V_{gs_M2}/V_T) \times (1 - \exp[-(V_{FD} - V_{pd})/V_T])$. For $V_{FD} - V_{pd} = V_T$, V_{gs_M2} must be increased by about $18mV$ relative to its original value when V_{FD} is at the reset level in order to maintain the same drain current. Thus the bias across the photodiode will be decreased by the same amount. Under uniform background illumination, the photocurrent of PD_{CM} is twice the photocurrent of an in-pixel photodiode, so the reverse bias voltage of an in-pixel photodiode is about $27mV$ greater than that of PD_{CM} . This helps to reduce the chance of any in-pixel photodiode becoming forward biased.

In addition to largely removing dark current and related artifacts, input referred noise arising from the readout circuits is reduced due to the large conversion gain resulting from the small capacitance C_{FD} of the floating diffusion region. The reset noise can be estimated from $\sqrt{kTC_{FD}/2}$. A low reset noise of $7e^-$ can be achieved with the C_{FD} of $0.58fF$ extracted from the layout.

In order to achieve good linearity, p-type transistors with separate nwells are used for the source follower input transistor M_{sf} and row select transistor M_{rsel} . The p-type source follower further increases the dynamic range by one V_{th} in comparison with conventional APS. The layout of two neighboring pixels is shown in Figure 3, where row select transistors in the two neighboring pixels share the same well. The pixel has an area of $5\mu m \times 5\mu m$, with a fill factor of 31%. A chip level reset-assist circuit, similar to the one described in [14], can be used to achieve the lower reset noise of soft reset without suffering the image lag associated with soft reset.

B. Column and chip level readout

A modified double delta sampling circuit (DDS) [15] is adopted for the readout. The column level circuits comprise one p-type loading transistor and two branches for sampling and storing the signal and reset levels. To enable video mode

operation without data interruption, an additional analog buffer stage is added to the column level sampling circuit. Therefore, while the data of one row stored in the second buffer are being read out column-wise, the signal and reset levels of pixels in the next row are sampled and stored in the first buffer. When the first column is selected again, signals for the next row are transferred to the second buffer. MOS capacitors of $150fF$ are used for both buffer stages. The signal swing range of $3.3V - V_{th}$ is maintained by alternately using n-type and p-type source followers. The input transistor of the n-type source follower is implemented in a pwell isolated from the p-type substrate using a deep nwell layer (DNW) and its source is connected to the pwell body. Therefore, the n-type source follower achieves good linearity as well. To reduce channel resistance and charge injection over the entire signal range, transmission gates with dummy transistors for both NMOS and PMOS are used for sample and hold switches connected to storage capacitors.

IV. SIMULATION RESULTS AND CHIP LAYOUT

Simulations confirm that the photodiode bias voltage will not vary significantly with the signal level at FD node. Figure 4 illustrates the source voltage of a common gate transistor as a function of its drain voltage while the gate voltage and drain current are held constant. The bias voltage across the photodiode changes less than $20mV$ for a signal swing of $1.8V$. In a pixel, the drain current is the sum of photocurrent and dark current, so it is expected to change slightly with the source voltage of the common gate transistor $M2$; however, this simple model represents the predominant effects.

The linearity of the analog signal chain including the in-pixel source follower is also confirmed by simulation. In order to quantify nonlinear effects in the readout chain, the output of the analog readout is subtracted from the ideal output with unity gain (i.e. the input value) and normalized by the amplitude of the input signal. A linearity better than 98% is achieved for input signals ranging from $0.3V$ to $2.1V$ as shown in Figure 5.

Sampling errors due to charge injection and clock feed through were also simulated. The offset between input and sampled signal is shown in Figure 6 as a function of signal level from $0.4V$ to $2.9V$. A loading capacitor of $200fF$ is used to account for the $150fF$ gate capacitance of MOS capacitor and parasitic capacitances introduced by the subsequent source follower and the switch itself. The offset for a transmission gate and single channel switch with dummy transistor are also shown for comparison.

To save chip area, $1.8V$ minimum size transistors are used for digital control blocks. A simple level shifter composed of a source follower and an inverter is used as the interface between control blocks and sensor array including pixel array and column-wise readout. All $1.8V$ digital components are built in deep nwells and a separate $3.3V$ power line is used for all level shifters. Thus, digital power and ground are separate from the analog power and ground in order to reduce coupling noise from the digital components.

V. SUMMARY

A new pixel structure for CMOS imagers has been described and analyzed. By adding one common gate transistor between the photodiode and integration node in a conventional three transistor one photodiode APS, a very large conversion gain can be achieved regardless of the photodiode area. As a result, both reset noise and input-referred read noise are significantly reduced. The gate voltage for all in-pixel common gate transistors is generated on chip to bias all photodiodes near zero volts. Dark current and its relevant artifacts are expected to be greatly improved. A modified DDS circuit is used to remove the FPN due to mismatch in column drivers. Switches in the column readout circuits are carefully designed so that charge injection and clock feedthrough noise are effectively suppressed over the entire signal swing range. With reduced noise and low dark current and good linearity, the image sensor is expected to be suitable for low-light applications.

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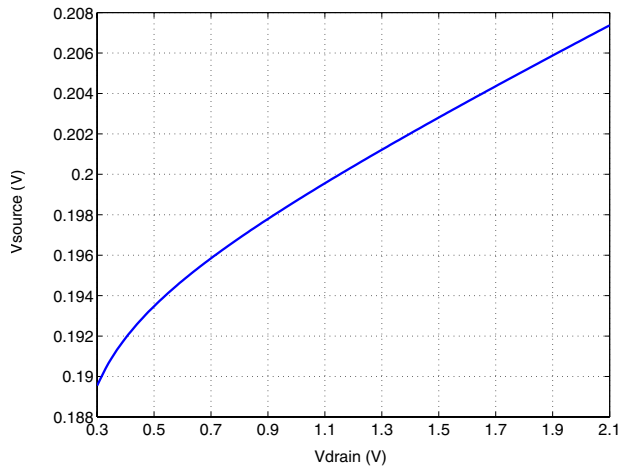


Fig. 4. Change in source voltage of a common gate transistor as a function of the drain voltage, where $I_{ds} = 1\text{pA}$ and $V_g = 0.5\text{V}$.

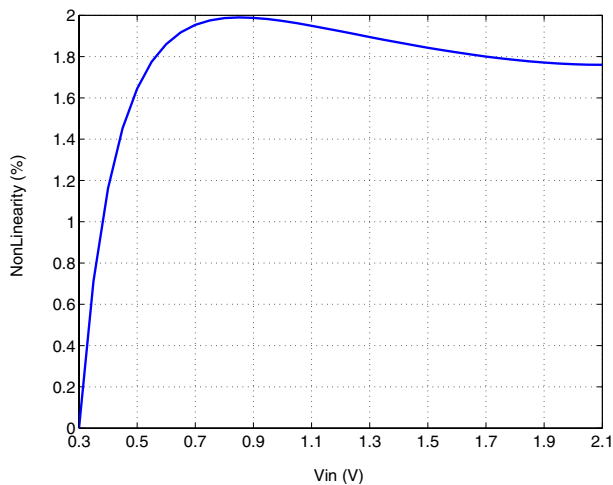


Fig. 5. Simulated linearity of the entire analog output chain including the in-pixel source follower.

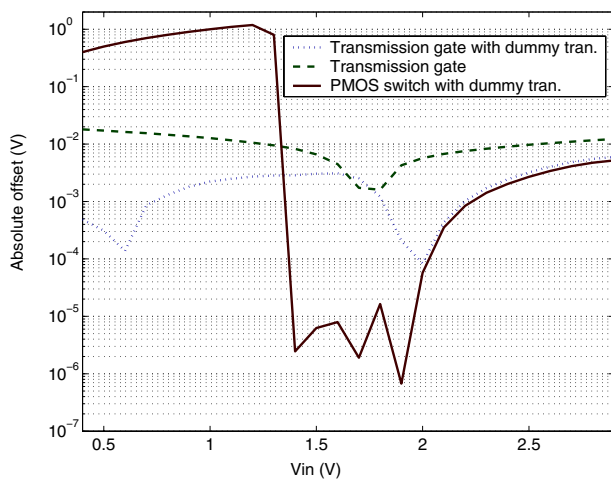


Fig. 6. Simulated offset between sampled signals and corresponding inputs of a sample and hold circuit, for implementations using three different switches.