

# **ENEE 719C: Mixed Signal VLSI Circuit Design**

Fall 2004

University of Maryland, College Park

Instructor:

Dr. Pamela Abshire

2211 A. V. Williams Bldg.

pabshire@umd.edu

(301) 405-6629

**Class times:** Lecture Tues Thurs 12:30-1:45pm CSI 2118

**Instructor Office Hours:** Tues 3-5pm in 2211AVW

**Course Website:** <http://umd.blackboard.com/>

## **Course Description**

This course is an advanced course on Mixed Signal VLSI design. We will review integrated circuits, devices, and deep sub-micron modeling. We will study the theory and design of mixed-signal circuits, including non-linear and switch analog, data conversion and interface circuits. The material involves extensive use of circuit simulation and layout CAD tools to design and verify circuits at various levels of abstraction, and draws upon knowledge from 400- and 600-level EE courses. Following current industry paradigms, students work in teams to design, thoroughly simulate, and specify physical layout of mixed signal VLSI circuits prior to their fabrication in a foundry. There will be a chip design project that can be submitted to MOSIS for fabrication.

## **Requisites**

Pre-requisite: ENEE 408B or ENEE 408D or equivalent and permission of instructor

## **Textbooks and Design Tools:**

*Required:*

Baker, Li and Boyce, *CMOS Circuit Design, Layout and Simulation*, 1997. (B I)

Baker, *CMOS Mixed Signal Circuit Design Vol II*, 2002. (B II)

*Strongly Recommended:*

S. Palnikar, *Verilog HDL, 2<sup>nd</sup> edition*, 2003.

*Tools:* Cadence Design Systems (Virtuoso, Spectre, Verilog-XL).

Students may also learn to use design tools such as MAGIC, PSPICE, HSPICE, and Tanner Tools (LEDIT, TSPICE).

## **Other useful references:**

- JHU Cadence Page: <http://bach.ece.jhu.edu/cadence/>
- Cadence Tutorial: <http://bach.ece.jhu.edu/cadence/manual/index.html>
- PSPICE Home Page: <http://www.orcadpcb.com/pspice/>
- MOSIS Home Page: <http://www.mosis.org/>
- Software and device models may be found on the class website.

**Topics:**

1. IC Devices
2. Scaling Issues
3. Deep Sub-micron SPICE Modeling, Layout and Verification
4. Non-linear Analog Circuits: Comparators, Adaptive Biases, Multipliers, Translinear Circuits
5. Dynamic Analog Circuits: Switched Capacitors, Clock Recovery Circuits, DLL, Asynchronous Digital Processing
6. Data Converter Fundamentals
7. Data Converter Architectures: ADC/DAC Architectures, Design and Performance
8. Read-out Electronics for Imaging Systems: Scanning Circuits, Correlated-Double Sampling, Video Sigma-Delta Modulators

**Grading:** The final grade will be based on class participation and presentations, two in-class exams, and a design project including complete written report, layout files, simulation results, and oral presentations. The following is a tentative weighting for determining overall grades: class presentations/participation 20%, exams 40%, project 40%.

**Class Participation/Presentations:** Supplementary material describing research relevant to the topics under study each week will be selected by the instructor and posted on the class website; students will be expected to present such material to the class twice during the semester. Although only one student is responsible for each presentation, all students are expected to discuss the material.

**Exams:** Your final score will be based in part on two exams. The dates for the exams will be announced in class at least one week in advance. Exam questions will be based on the material covered in class.

**Projects:** The project requirements and deliverables will be described in class. Students may form teams, propose appropriate design problems, partition and distribute design tasks among teams and within each team. Students are responsible for providing complete written reports, including layout files, analysis and simulation results and accounts of individual contributions by team members. Suggested research topics include:

- Capacitive sensing / imaging of physical contact
- Bioimaging / imaging of cells for cell steering or monitoring
- Address event imaging
- High resolution amperometric potentiostat with ADC
- Low power, short range RF wireless communication
- Short range UV communication

**Office Hours:** Please come during regular office hours (Tues 3-5pm). Other times are fine, but by appointment ONLY.

**Course Materials Distribution:** While some of the course material will be distributed in lecture, most course material will be available from the class website. In the beginning of the course, I will attempt to verify that class notifications are reaching your email address; however, it will be your responsibility to ensure continued receipt of class information. All class announcements will be posted onto the class website as an alternative means of retrieving updated information.

**Absences:** It is my intent to respect our diverse community's religious observances, so please inform me in writing (email) of any intended absences for religious observances in advance. Notice should be provided as soon as possible but no later than the end of the second week of classes.

**Academic Integrity:** Although I am not expecting to encounter this issue, I would like to make it very clear that academic dishonesty will not be tolerated. All work submitted for grading must be your own. Academic dishonesty in this class includes outright copying of homework or electronic material or deliberately taking unfair advantage of other students in the class; however, discussing homework and projects is permissible and also encouraged.

**Tentative Schedule:**

Week 1 (Aug 31, Sep 2): Background Review, Cadence Intro, BI 1-5, 7, 9-10  
Week 2 (Sep 7, 9): Scaling Issues, Deep Sub-micron Modeling, BI-6, BII-34  
Week 3 (Sep 14, 16): Nonlinear Analog Circuits, BI-26  
(Comparators, Adaptive Biases)  
Week 4 (Sep 21, 23): Nonlinear Analog Circuits, BI-26  
(Multipliers, Translinear Circuits)  
Week 5 (Sep 28, 30): Dynamic Analog Circuits, BI-27  
(Switched Capacitors, Clock Recovery, Delay Locked Loop)  
Week 6 (Oct 5, 7): Dynamic Analog Circuits, BI-27  
(Asynchronous Digital Processing)  
Week 7 (Oct 12, 14): Data Converter Fundamentals, BI-28; *Exam 1*  
Week 8 (Oct 19, 21): Data Converter Fundamentals, BII 30-32  
Week 9 (Oct 26, 28): Data Converter Architectures (ADC/DAC), BI-29  
Week 10 (Nov 2, 4): Data Converter Architectures (ADC/DAC), BII-35  
Week 11 (Nov 9, 11): CMOS Imagers  
Week 12 (Nov 16, 18): Readout Electronics for Imagers  
(Scanning Circuits, Correlated Double Sampling, Video Sigma-Delta Modulators)  
Week 13 (Nov 23): Readout Electronics for Imagers, cont'd.  
*Nov 25 is Thanksgiving holiday*  
Week 14 (Nov 30, Dec 2): Advanced Topics; *Exam 2*  
(TBD. Possible topics include power & noise, biomorphic systems, adaptive circuits, floating gate circuits, ...)  
Week 15 (Dec 7, 9): Advanced Topics, cont'd.  
Week 16 (Dec 17): Final Presentations 1:30-3:30pm