

# Capstone Design Project: Mixed Signal VLSI Design

## ENEE 408D, Spring 2007

University of Maryland, College Park

Instructor:

Dr. Pamela Abshire  
2211 A. V. Williams Bldg.  
pabshire@umd.edu

(301) 405-6629

TAs:

Alfred Haas, Nicole Nelson  
2160 A. V. Williams Bldg.  
{ahaas@umd.edu,  
nmnelson@glue.umd.edu}

(301) 405-8974

**Class times:** Lecture Mon Wed 10:00-11:15pm JMP 3201  
Lab Fri 10:00-10:50am, 1:00-1:50pm EAB 0305

**Instructor Office Hours:** TBA

**TA Office Hours:** TBA

**Course Website:** <http://bb.eng.umd.edu/>

**Course Description:** This course covers the design of very large scale integrated (VLSI) circuits, including analysis and simulation of digital and analog circuits, layout, and component selection. The material involves extensive use of circuit simulation and layout CAD tools, and draws upon knowledge from 300-level EE courses. Following current industry paradigms, students work in teams to design, thoroughly simulate, and specify physical layout of mixed signal VLSI circuits prior to their fabrication in a foundry.

**Required Text:** R. J. Baker, *CMOS Circuit Design, Layout and Simulation*, 2<sup>nd</sup> ed., 2005.

**Required Design Tools:** Tanner Tools (L-EDIT and TSPICE) and PSPICE.  
Students may also learn to use design tools such as MAGIC, Cadence, and HSPICE.

### Other useful references:

- Physical Operation of the P-N Junction, Diodes, and Transistors, Jon Orloff (e-text available on class website)
- Tanner EDA Home Page: <http://www.tanner.com/EDA/>
- PSPICE Home Page: <http://www.orcad.com/pspicead.aspx>
- MOSIS Home Page: <http://www.mosis.org/>
- Textbook Home Page: <http://cmosedu.com/cmos1/book.htm>
- Software and device models may be found on the class website.

**Prerequisites:** ENEE 302, ENEE 306, ENEE 312 and permission of instructor.

**Grading:** Your final grade will be based on homework, a mid-term exam, a final exam, and a term project including complete written reports, layout files, simulation results, accounts of individual contributions by team members, and oral presentations. The following is a tentative

weighting for determining overall grades: final exam 15%, midterm 10%, project 50%, homework 25%.

**Course Objectives:** The objectives of this class are to develop an understanding of the design of very large scale integrated (VLSI) circuits. Students will use background from this class and others to propose, design, analyze, simulate, and layout a mixed-mode VLSI circuit project. Students are expected to:

- Consolidate and apply key concepts in semiconductor devices, analog circuits and digital circuits, introduced earlier in the electrical and computer engineering curricula;
- Select appropriate design problems, partition and distribute design tasks among student teams and within each team;
- Analyze and design complex CMOS integrated circuits including: DC, transient and small signal responses of (i) simple and cascode current mirrors, (ii) CMOS basic and cascode op-amps;
- Design complex circuits for optimal phase margin, gain, frequency response trade-offs;
- Design digital circuits for optimal fan-out, minimum propagation delay;
- Use circuit simulators such as SPICE in detail;
- Use layout tools to implement circuit designs on a silicon chip; and
- Understand how semiconductor physics influences chip design rules and sets limits on integrated circuit performance.

**Topics Covered:** This course is an introduction to modern integrated circuit design. The topics covered include:

- Economic motivation for IC circuit fabrication
- Environmental issues in chip fabrication; use and disposal of dangerous chemicals
- CMOS IC design and fabrication; the IC layout program LASI
- Designing and laying out the integrated circuit well
- Metal layers, pads, and interconnects
- Design and layout of active and polysilicon layers
- MOSFET design, fabrication, and operation
- Parasitic elements due to layout and device structure, and the resulting RC delay and inductive cross talk
- Digital CMOS circuits: the operation and layout of the inverter, nand, and, nor gates
- Advanced SPICE modeling
- Analog CMOS circuits: the operation and layout of current sources, differential amplifiers, active loads, cascode loads, operational amplifiers, frequency compensation, operational transconductance amplifiers
- Mixed-signal circuits for specific applications (e.g., communications)
- Design optimization: minimum propagation delay, optimal fan-out

**Homework:** Homework is due by the end of class/lab on the assigned date. They will be distributed from the class website. Electronic files will be accepted on the class website (*Digital Dropbox*). Late homework may be accepted at the discretion of the instructor and grader but will suffer grading penalties. Late homework must be submitted electronically, delivered to me in my office or slid under the door. Do not put them in my mailbox. Please staple your

assignments together; I will not take responsibility for lost sheets. If you go by another name than the one officially registered with the University, please write both names down for the first few assignments. While I encourage you to discuss course material with other students, the homework problems are to be completed independently. If your homework appears to be identical to another student's, you will receive no credit for the assignment and you may be asked to demonstrate your understanding of the material to the instructor or TA in an oral quiz. Homework solutions that are not legible will not be graded.

**Exams:** Your final score will be based in part on a midterm exam and a final exam. The dates for the midterm and final will be announced in class at least one week in advance. Makeup exams are only possible for those with officially documented excuses (i.e. approved by the undergraduate studies office). Exam questions will be based on the material covered in class. All work for long answer questions must be shown in order to receive full credit.

**Projects:** The project requirements and deliverables will be described in class. Students will complete a group project and are expected to form teams, propose appropriate design problems, partition and distribute design tasks among teams and within each team. Student teams are responsible for providing complete written reports, including layout files, analysis and simulation results and accounts of individual contributions by team members. Each team is required to deliver an oral presentation describing their project. Students will present their projects during a **class mini-symposium** (to be scheduled) The mini-symposium will last approximately three hours and will take the place of a final examination. All students are required to attend the entire symposium.

**Office Hours:** Please come during regular office hours (TBA). Other times are fine, but by appointment ONLY. Questions about the homework, grading, or the material presented in class should be first directed to the TA.

**Course Materials Distribution:** While some of the course material will be distributed in lecture, supplementary course material will be available from the class website. It will be your responsibility to ensure continued receipt of class information. All class announcements will be posted onto the class website as an alternative means of retrieving updated information.

**Absences:** It is my intent to respect our diverse community's religious observances, so please inform me in writing (email) of any intended absences for religious observances in advance. Notice should be provided as soon as possible but no later than the end of the second week of classes.

**Academic Integrity:** Although I am not expecting to encounter this issue, I would like to make it very clear that academic dishonesty will not be tolerated. All work submitted for grading must be your own. The University of Maryland, College Park has a nationally recognized Code of Academic Integrity, administered by the Student Honor Council. This Code sets standards for academic integrity at Maryland for all undergraduate and graduate students. As a student you are responsible for upholding these standards for this course. It is very important for you to be aware of the consequences of cheating, fabrication, facilitation, and plagiarism. For more

information on the Code of Academic Integrity or the Student Honor Council, please visit <http://www.studenthonorcouncil.umd.edu/whatis.html>.

**Tentative Schedule:**

Dates	Read	Topic	Due	Lab
Wk 1 (Jan 24, 26)	Ch 1	Intro and Review		Lecture + Intro to Tanner Tools
Wk 2 (Jan 29, 31, Feb 2)	Ch 2 and 3	Nwell and Metal Layers; Parasitics	HW1	Project Ideas
Wk 3 (Feb 5, 7, 9)	Ch 4	.	HW2	Project Ideas
Wk 4 (Feb 12, 14, 16)	Ch 5 and 6		Project Description	Design Rules
Wk 5 (Feb 19, 21, 23)	Ch 9 and 10		Lit Review	Design Rules
Wk 6 (Feb 26, 28, Mar 2)	Ch 11		Block Diagram	
Wk 7 (Mar 5, 7, 9)	Ch 12		HW3	
Wk 8 (Mar 12, 14, 16)	Ch 12	Midterm Exam	Schematic and Analysis	
Wk 9 (Mar 19, 21, 23)		Spring Break		
Wk 10 (Mar 26, 28, 30)	Ch 13		HW4	
Wk 11 (Apr 2, 4, 6)	Ch 9		Simulations	
Wk 12 (Apr 9, 11, 13)	Chs 20 and 21		Design Review	Design Review
Wk 13 (Apr 16, 18, 20)	Ch 22		HW5	
Wk 14 (Apr 23, 25, 27)	Ch 24			
Wk 15 (Apr 30, May 2, 4)	Ch 25		Layout	
Wk 16 (May 7, 9)		Final Exam		
May ??		Class Conference	Final Presentation and Report	