

# A Floating-Gate Comparator With Automatic Offset Adaptation for 10-bit Data Conversion

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**Abstract**—We present a novel voltage comparator that uses nonvolatile floating-gate charge storage for either offset nulling or automatic programming of a desired offset. We exploit the negative feedback mechanism of pFET hot-electron injection to achieve fully automatic offset cancellation. The adaptation guarantees an input offset less than the input-referred noise level regardless of initial device offset for a typical 8.3% observed injection mismatch. In addition, we demonstrate the ability to accurately program a desired offset. The design has been fabricated in a commercially available 0.35- $\mu\text{m}$  process. Experimental results confirm the ability to reduce the variance of the initial offset by two orders of magnitude and to accurately program a desired offset with maximum observed deviation 728  $\mu\text{V}$  and typical deviation 109  $\mu\text{V}$ . The mean offset is reduced by a factor of 416 relative to fabricated chips directly from the foundry and by a factor of 202 relative to UV-irradiated chips. Adaptation is fast, with settling time typically under 50 ms and scaling inversely with the exponential of the injection voltage. We achieve controlled injection to accurately program the input offset to voltages uniformly distributed from  $-1$  to  $1$  V. The comparator exhibits a 5 ns propagation delay and consumes 270  $\mu\text{W}$ .

**Index Terms**—Adaptive systems, analog–digital conversion, analog memories, calibration, CMOS integrated circuits, comparators, floating gate, hot carriers, offset cancellation, very large-scale integration (VLSI).

## I. INTRODUCTION

COMPARATORS are decision-making circuits that interface between analog and digital signals. Comparators are used in a wide variety of circuit applications, including analog-to-digital converters, memories, dynamic logic, and sense amplifiers. A comparator usually consists of a pre-amplifier stage and a regenerative stage followed by a buffer. Mismatches due to process variation in the pre-amplifier and regenerative stages cause offset that directly affects resolution. A common and successful approach used to cancel offset is dynamic switching [1], which requires additional circuit

components and multiple nonoverlapping clocks. We report an adaptation method that requires a single switch and one clock signal to either program or cancel an offset. Since offset is a property of the circuit, it is natural to store it using nonvolatile storage on a floating gate. Floating-gate circuits have been used to cancel offsets in imagers [2], to trim current sources [3]–[5], and to autozero amplifiers [6], [7]. The ability to program desired nonzero offsets in comparators is a feature that is not readily available using existing offset cancellation techniques but is intrinsic to the voltage comparator we describe here.

We present the design of a comparator that automatically and accurately cancels offset, or depending on the application, can store a predetermined offset [8]. The offset may be cancelled or programmed in either a one-shot or continuous fashion to calibrate for constant or changing conditions; the offset is retained using nonvolatile local storage, and for certain applications it is not necessary to recalibrate dynamically. The calibration mechanism is self-limiting and converges to a stable value without user intervention. In Section II, we discuss methods for manipulating charge on floating-gate nodes. In Section III, we introduce a novel adaptive circuit that uses nonvolatile charge storage to achieve accurate, fast voltage comparison. We discuss two calibration methods and compare their effectiveness both analytically and experimentally. We also analyze the design tradeoff between resolution and speed for this circuit. We use Monte Carlo simulations in HSPICE to compare the input offset distributions of a comparator without floating-gate transistors to those of a comparator with floating-gate offset cancellation before and after calibration. In Section IV, we present detailed experimental results on calibration accuracy, conversion accuracy, offset distribution before and after calibration, and the time course of calibration. We report statistical parameters for injection mismatch and the bias dependence of injection time constant as determined from empirical measurements.

## II. BACKGROUND

A floating-gate MOSFET uses an electrically isolated material as its gate. There are no direct electrical connections to this circuit node, so charge on this gate remains trapped for a very long time. Offset correction for the comparator reported in this paper is stored in this high-retention charge form, and altered by means of injection.

The impact-ionized hot-electron injection mechanism has been extensively described in the literature [7], [9], and the injection feedback mechanisms for both nFET and pFET are discussed in detail in [10]. We briefly summarize the pFET injection feedback mechanism. For pFET injection, a constant current configuration exhibits negative feedback from the drain voltage to the floating-gate voltage, which drives the floating

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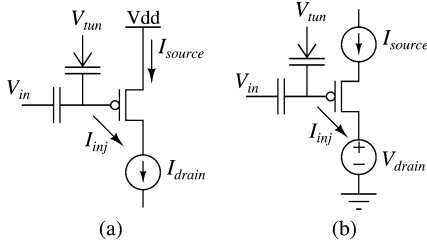


Fig. 1. Injection current exhibits negative feedback in the pFET constant current configuration in (a) the autozeroing amplifier [6] and (b) the *gate follower* used in the AFGC.

gate to a stable operating point. Fig. 1(a) is the configuration used in the autozeroing amplifier [6], and Fig. 1(b) is the *gate follower* configuration we use in this comparator. They are both constant current configurations.

With the thin oxides, small feature sizes, and high doping concentrations in modern processes, injection can occur at voltages less than or equal to  $V_{dd}$ . An accurate empirical model in [11] suggests that injection produces a current  $I_{inj}$  from the floating gate into the channel

$$I_{inj} = \alpha I_s \exp \left[ -\frac{\beta}{(V_{gd} + \delta)^2} + \lambda(V_{gd} - V_{gs}) \right] \quad (1)$$

where  $I_s$  is the source current,  $V_{gd}$  and  $V_{gs}$  are gate-to-drain and gate-to-source voltages, and  $\alpha$ ,  $\beta$ ,  $\lambda$ ,  $\delta$  are empirically determined parameters. The current  $I_{inj}$  scales as an exponential function of gate-to-drain voltage  $V_{gd}$ . When  $V_{gd}$  increases, injection current  $I_{inj}$  also increases. The flow of electrons onto the floating gate decreases the gate voltage and reduces  $V_{gd}$ . In a constant current configuration, the source voltage adjusts so that  $V_{gs}$  is approximately fixed. With  $V_{gs}$  fixed, injection proceeds to decrease the gate voltage until it reaches a value where the injection current stops. This negative feedback configuration causes the gate voltage to follow the drain voltage; hence the name *gate follower*. We use the *gate follower* configuration for the input pFET differential pair in our comparator which couples the output voltages to the input floating-gate voltages to realize output offset storage [1] for offset nulling.

Injection of electrons onto the floating gates of pFETs is a one-way process that lowers the voltages of the floating nodes. When used in a differential signal representation, these one-way increments can store both positive and negative offsets. However, the injection currents always decrease the common-mode voltage of the floating nodes monotonically, and we must ensure that the common-mode voltage remains in a reasonable range for circuit operation. If necessary, this can be achieved using a tunneling current [12] onto the floating-gate nodes to increase the common-mode voltage. Together, the two mechanisms, injection and tunneling, can achieve voltage shifts in both directions to reach a desired input common-mode voltage: first, tunneling is used to raise the common-mode voltage using a separate tunneling electrode, or through the pFET's gate oxide; then injection is used to calibrate the input offset voltage. This two-step procedure sets a desired input offset and a desired common-mode voltage at the same time. However, we have found that the initial tunneling step is not necessary in practice, and all experimental results (Section IV) have been obtained by UV irradiation followed by injection, without an extra tunneling

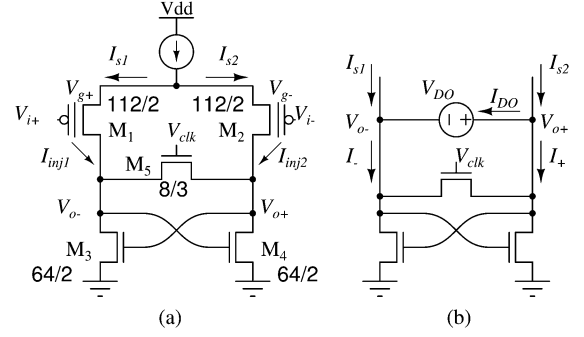


Fig. 2. AFGC. (a) Circuit diagram of the AFGC with pFET input floating-gate differential pair, crosscoupled nFET regenerative elements, and reset switch. Dimensions are specified as width/length, with unit  $\lambda = 0.2 \mu\text{m}$ . The coupling capacitors from inputs  $V_{i+,-}$  to floating gates  $V_{g+,-}$  are 216 fF. (b) During evaluation, bias voltage  $V_{clk}$  on the reset switch  $M_5$  determines conductance of the regenerative elements and overall comparator gain. Transconductance of the crosscoupled pair and switch is determined using HSPICE simulation of circuits extracted from layout, as described in the text.

step. The adaptation methods described in Section III achieve common-mode voltages that are suitable for circuit operation using only injection.

The integrated circuit implementation described in this paper has been fabricated in a technology which provides linear capacitors between polysilicon layers. For ease of implementation, this linear capacitor has been used to implement the capacitive coupling from the input nodes onto the floating-gate nodes. Further, we use the top polysilicon layer poly-2 as the floating node rather than poly in order to minimize parasitic capacitances to ground. The floating node is connected to the gate of a pFET transistor via metal-1. The circuit described below does not require linear capacitance and may be implemented using nonlinear MOS capacitors. Thus, the circuit is compatible with standard digital CMOS processes; we intend to demonstrate this compatibility in future implementations of the adaptive floating-gate comparator (AFGC).

### III. ADAPTIVE FLOATING-GATE COMPARATOR

The simple five-transistor circuit shown in Fig. 2(a) implements the AFGC, comprising pre-amplification and regenerative stages for the comparison as well as control and local storage for the adaptation. During normal operation (adaptation disabled), floating-gate transistors  $M_1$  and  $M_2$  form the input devices of a differential pair and provide local charge storage. Cross-coupled nFET transistors  $M_3$  and  $M_4$  form the regenerative elements of the comparator. When the clock signal  $V_{clk}$  is “high,” the nFET switch  $M_5$  closes and resets the comparator. When  $V_{clk}$  is low, switch  $M_5$  opens and the evaluation phase begins. The “high” bias voltage on transistor  $M_5$  during reset determines conductance of the regenerative elements and thereby the overall gain and speed of the comparator.

With the power-supply  $V_{dd}$  set at the nominal operating voltage of 3.3 V, there is insufficient electric field between the pFET's drain and source to produce hot electrons in the channels of  $M_1$  and  $M_2$ . We therefore keep the AFGC's  $V_{dd}$  at 4.5 V during both normal operation and adaptation.  $V_{dd} = 4.5 \text{ V}$  strengthens source-to-drain electric fields thereby increasing the energy of electrons in the channels of  $M_1$  and  $M_2$ . Adaptation is controlled by the common-mode input

voltage  $V_{CM}$ : the common source voltage will follow  $V_{CM}$ , so raising  $V_{CM}$  enables adaptation by increasing the gate-to-drain and source-to-drain electric fields thus attracting hot electrons onto the floating gate. Conversely lowering  $V_{CM}$  disables adaptation by decreasing the source-to-drain and gate-to-drain electric fields so that fewer hot electrons are generated and so that fewer hot electrons are collected on the floating gate. During adaptation, negative charges accumulate on each of the floating gates, lowering their gate-to-drain and source-to-drain voltages and establishing negative feedback between the outputs and the inputs to achieve stable adaptation. While the adaptation mechanism for the AFGC results in reduction in the common-mode voltage on the floating nodes, all results reported in this work include any additional error resulting from this shift; thus it does not present a significant limitation to accurate and automatic adaptation.

In Sections IV-A–D, we discuss two methods of injection, a static method and a dynamic method. The static method is simple and serves to illustrate the mechanism of calibration, but its accuracy is limited in practice. The dynamic injection method overcomes the accuracy limitations of the simple static method and provides calibration accuracy under 1 mV; however, during dynamic injection the adaptation occurs during the evaluation phase so the output of the comparator is latched. This means that the update direction cannot change during a single cycle, thus accurate calibration must be achieved over many clock cycles. We also discuss the inherent tradeoffs between speed and accuracy, which can be tuned using the clock voltage  $V_{clk}$ . We present Monte Carlo simulations and experimental results which demonstrate the efficacy of calibration using the dynamic injection method.

#### A. Static Injection Method

The static injection method accomplishes adaptation by applying a constant voltage bias to the clock terminal. When the clock is high, the comparator becomes an amplifier whose differential inputs ( $V_{i+} - V_{i-}$ ) and differential outputs ( $V_{o+} - V_{o-}$ ) are related by a finite voltage gain  $A_V = ((V_{o+} - V_{o-}) / (V_{i+} - V_{i-})) = cA_{fg}$ . The constant  $c$  is the capacitance ratio  $C_{fg} / C_T$ , where  $C_{fg}$  is the capacitance between nodes  $V_{i+}$  and  $V_{g+}$  (and between nodes  $V_{i-}$  and  $V_{g-}$ ), and  $C_T$  is the total capacitance coupled to the floating node  $V_{g+}$ . The voltage gain  $A_{fg}$  from floating nodes  $V_{g+}$  and  $V_{g-}$  to the differential outputs is greater than the overall voltage gain  $A_V$ . The goal of offset cancellation is to balance the differential output ( $V_{o+} = V_{o-}$ ) when the input difference is zero ( $V_{i+} = V_{i-}$ ). Suppose that mismatch causes the outputs to be unbalanced ( $V_{o+} > V_{o-}$ ) when the inputs are equal. When Vdd is sufficiently high, injection occurs when the common-mode input voltage  $V_{CM} = (V_{i+} + V_{i-})/2$  is raised. Since the source-to-drain voltage of  $M_1$  is greater than that of  $M_2$ , the injection current  $I_{inj1}$  onto the floating gate of  $M_1$  will be greater than the injection current  $I_{inj2}$  at  $M_2$  and the floating-gate potential  $V_{g+}$  will decrease faster than  $V_{g-}$ . As a result, the differential current  $I_{s1}$  will increase with a concomitant decrease in  $I_{s2}$ , causing the output voltage  $V_{o-}$  to rise and  $V_{o+}$  to fall. This feedback cycle will drive the floating-gate voltages  $V_{g+}$  and  $V_{g-}$  to values that compensate for the initial device mismatches.

The input-referred offset after calibration depends on Early voltage, voltage gain and mismatch of both device and injection parameters. The voltage gain  $A_{fg}$  is the product of the input transconductance and the equivalent output resistance ( $A_{fg} = g_{m12}R_{eq}$ ), where  $R_{eq} = [r_{o12} \parallel r_{o34} \parallel (g_{m5} + g_{m34})^{-1}]$ . We define conductance and resistance differentially, e.g.,  $g_{m12} = \partial(I_2 - I_1) / \partial(V_{g+} - V_{g-})$  and  $r_{o12} = \partial(V_{o+} - V_{o-}) / \partial(I_1 - I_2)$ , where  $I_1$  and  $I_2$  represent the channel currents of  $M_1$  and  $M_2$ , respectively. Note that for the positive feedback pair  $M_3$  and  $M_4$ , the conductance  $g_{m34} < 0$ . Suppose that there is an initial output offset  $V_{o+} - V_{o-} = \Delta V_o > 0$  when  $V_{i+} = V_{i-}$  and  $V_{g+} = V_{g-}$  (i.e., the inputs are equal and there is no charge on the floating gate). Injection causes  $V_{g+}$  to decrease by  $\Delta V_{i+}$  and  $V_{g-}$  to decrease by  $\Delta V_{i-}$ , so the differential output becomes  $\Delta V'_o = V'_{o+} - V'_{o-} = (V_{o+} - V_{o-}) + A_{fg}(\Delta V_{i-} - \Delta V_{i+})$ .

The adaptation reaches equilibrium when both sides of the differential pair are decremented equally. Imbalance can result from mismatch of capacitance on the floating gates, mismatch of injection parameters, mismatch of Early voltage, or mismatch in bias conditions between the two sides of the differential pair. In the following development, we assume matched capacitances, injection, and Early voltage, and focus on the bias dependence. In this case adaptation is complete when the injection currents reach the same magnitude  $I_{inj1} = I_{inj2}$ . The time required to achieve equilibrium is a function of initial offset (see Section IV-D), so in practice we simply let the system continue injecting for some fixed time. As injection continues, the floating-gate voltages and the common source voltage continue to decrease, so the source-to-drain voltages and gate-to-drain voltages decrease and the two injection currents eventually decrease to zero  $I_{inj1} = I_{inj2} \rightarrow 0$ . Equilibrium is attained when the currents balance and it is not necessary to wait for them to approach zero. Under the operating conditions described, the dominant term in the exponent of (1) is a nonlinear function  $f_1(\cdot)$  of gate-to-drain voltage  $V_{gd}$ , so we approximate (1) as  $I_{inj} = \alpha I_s e^{f_1(V_{gd})}$ . Assuming matched injection parameters  $\alpha$  and  $I_s$

$$\alpha I_s e^{f_1[(V_{g+} - \Delta V_{i+}) - V'_{o-}]} = \alpha I_s e^{f_1[(V_{g-} - \Delta V_{i-}) - V'_{o+}]},$$

Therefore  $\Delta V'_o = V'_{o+} - V'_{o-} = \Delta V_{i+} - \Delta V_{i-} = \Delta V_o - A_{fg}(\Delta V_{i+} - \Delta V_{i-})$ , and  $\Delta V_o = (\Delta V_{i+} - \Delta V_{i-})(1 + A_{fg})$ , so the input-referred offset after injection is

$$\Delta V'_i = \frac{\Delta V'_o}{A_{fg}} = -\frac{\Delta V_o}{A_{fg}(A_{fg} + 1)}.$$

The input-referred offset will be reduced by  $(A_{fg} + 1)$  after adaptation. Although we assumed initial matched gate voltages  $V_{g+} = V_{g-}$ , this is not required. We can consider an initial gate offset  $V_{g+} - V_{g-} = \Delta V_g$  as part of the input offset, which produces an extra term  $A_{fg}\Delta V_g$  in the initial output  $\Delta V_o$ . As adaptation reaches equilibrium, this extra term in the output is eliminated and the net result is the same.

To make the gain as high as possible, we bias  $V_{clk}$  so that the conductance  $g_{m5} + g_{m34}$  is reduced to a small positive value. Note that  $g_{m5} + g_{m34} = (I_+ - I_-) / (V_{o+} - V_{o-})$ . We find this operating point from HSPICE simulation of a circuit extracted from layout using the configuration shown in Fig. 2(b). We set equal currents in the two sides of the differential pair

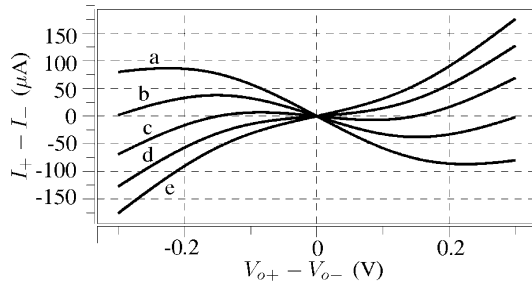


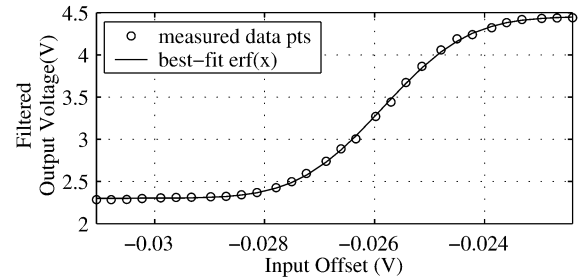
Fig. 3. Bias voltage  $V_{\text{clk}}$  controls the conductance of the switch and regenerative crosscoupled pair. Simulated current-voltage relationship for the circuit of Fig. 2(b) for  $V_{\text{clk}}$  from (a) 1.4 V to (e) 3 V in 0.4 V steps.

( $I_{s1} = I_{s2}$ ) by applying equal gate voltages, and introduce an offset voltage source  $V_{DO}$  between  $V_{o+}$  and  $V_{o-}$ . We plot the current difference  $-2I_{DO} = I_+ - I_-$  as a function of the voltage difference  $V_{o+} - V_{o-}$  in Fig. 3. The conductance  $g_{m5} + g_{m34}$  depends on  $V_{\text{clk}}$  and can be found from the slope of the curves at the origin. Negative  $g_{m5} + g_{m34}$  causes positive feedback during reset and results in hysteresis in the circuit behavior. Negative  $g_{m5} + g_{m34}$  occurs for low clock voltages ( $V_{\text{clk}} \leq 2.2$  V, e.g., traces a, b and c). In order to maximize the gain  $A_{fg}$  and avoid hysteresis,  $V_{\text{clk}}$  is selected so that  $g_{m5} + g_{m34}$  is positive ( $V_{\text{clk}} = 2.6$  V in trace d of Fig. 3).

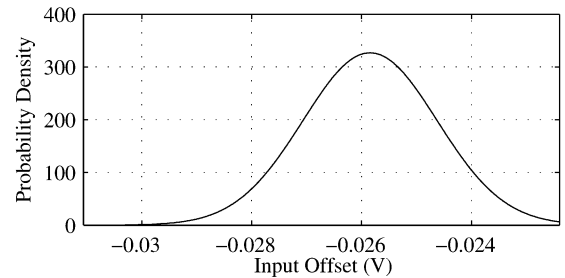
While the method of static injection described above may be used successfully to decrease offsets, its ability to accurately cancel offsets is limited in practice. Both simulation and experiment (see Fig. 15, shown later) demonstrate the phenomenon of “overshoot”—that is, injection does not stop when  $V_{o+} = V_{o-}$ , resulting in an equilibrium with  $V_{o+} < V_{o-}$  when injection currents are balanced. This overshoot phenomenon exists because the injection currents become unbalanced during programming. The injection currents are proportional to the channel currents of the pFET differential pair, and these currents are changing in value due to adaptation. Note that the equilibrium does not imply equal channel currents or equal output voltages, since injection depends on both channel current and gate-to-drain voltage. Mismatch in injection, floating node capacitance, or Early voltage will further limit the accuracy of static injection.

### B. Dynamic Injection on the Floating Gates

We describe a dynamic injection technique which overcomes the overshoot problem observed when using static injection. The dynamic technique achieves injection during the evaluation phase when the clock signal  $V_{\text{clk}}$  is low and the comparator is latched, with adaptation achieved over many evaluation cycles. By injecting with a running clock, we use the outcome of each comparison to correct offset during the corresponding evaluation cycle. Thus, the feedback loop encompasses all mismatch and offset within the circuit, and accurate offset cancellation can be achieved. We bias the common-mode input voltage  $V_{\text{CM}}$  so that the drain-to-channel voltage is insufficient for injection during the reset phase of the clock cycle, but sufficient to produce injection during the evaluation phase when one of the outputs  $V_{o+}$  or  $V_{o-}$  is close to ground. From a simulation model [11] and our own experimental results, injection begins when drain-to-channel voltage exceeds 3 V. For a pFET



(a)



(b)

Fig. 4. Circuit noise causes uncertainty in the outcome of the comparison. (a) Typical input offset distribution for one device obtained experimentally, showing measured voltage distribution and empirically fitted error function. (b) Corresponding empirical Gaussian probability density function.

threshold of 1 V, we bias  $V_{\text{CM}}$  above 2 V. During reset both outputs are clamped at approximately the threshold voltage of an nFET  $V_{o+} \approx V_{o-} \approx 0.7$  V, so we set the desired  $V_{\text{CM}}$  between 2 V and 2.7 V. For  $V_{\text{CM}}$  higher than 2.7 V, injection initially occurs during both reset and evaluation, but quickly reduces the common-mode voltage of the floating nodes to 2.7 V, after which the circuit enters the desired operating range. Suppose that the initial mismatch causes the outputs to be unbalanced  $V_{o+} > V_{o-}$  when inputs are equal. When the comparator latches,  $V_{o-}$  is pulled to ground, injecting a small charge  $Q_{\text{inj}}$  on the gate  $V_{g+}$ . The charge accumulates on gate  $V_{g+}$  for each clock cycle until the gate voltage is low enough that the outcome reverses ( $V_{o+} < V_{o-}$ ). Thereafter, the outcome alternates for each cycle and causes injection on the opposite side of the p-differential pair. Adaptation is controlled by the outcome of the comparison and the offset can be finely tuned.

In practice, any comparator has a limited conversion accuracy that can be defined by the variance of the input-referred noise. Ambiguity exists near the switching point where the outcome is uncertain. This uncertainty is caused by flicker noise and thermal noise generated by the MOSFETs within the circuit. The probability that the outcome is correct depends on how far the input is away from the switching point. Empirically, we find that this distribution is Gaussian, so we characterize the distribution with the mean and standard deviation obtained from the measured data. Fig. 4 shows a typical measurement from one AFGC circuit. Fig. 4(a) plots the measured comparison outcome as a function of the differential input voltage  $V_d = V_{i+} - V_{i-}$  with an empirically fitted error function. This outcome is determined by observing the actual outcome through a low-pass filter [see Fig. 10(b), shown later, and detailed description in Section IV], and can be transformed to the cumulative distribution function (cdf) of the actual outcome through normalization. Fig. 4(b) shows the probability density function (pdf) cor-

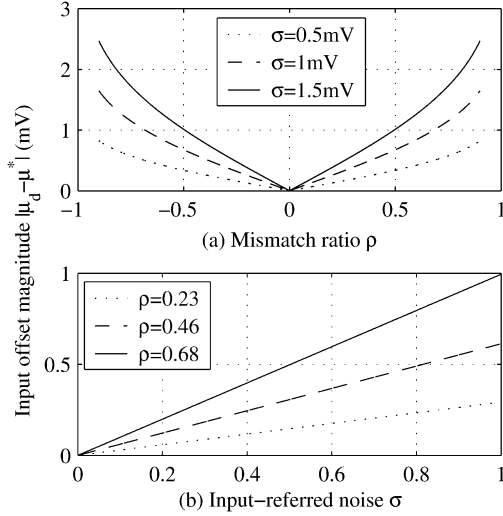


Fig. 5. Absolute value of the input offset  $|\mu_d - \mu^*|$  after calibration according to (2): (a) as a function of  $\rho$  for several values of  $\sigma$ , and (b) as a function of  $\sigma$  for several values of  $\rho$ .

responding to the fit with mean  $\mu = -25.9$  mV and standard deviation  $\sigma = 1.1$  mV.

Let  $X$  be a random variable representing the actual input offset having a nonzero mean  $\mu$  and variance  $\sigma^2$ . Then the cdf obtained from Fig. 4(a) corresponds to  $P[X < V_d]$ . The goal of adaptation is for  $\mu$  to approach a desired offset  $\mu_d$ . Using the dynamic injection method, during each clock cycle  $\mu$  increases by  $\Delta V_1 = C_1^{-1} \int_T I_{inj1} dt \approx Q_{inj1}/C_1$  for  $X < \mu_d$ , and decreases by  $\Delta V_2 \approx Q_{inj2}/C_2$  for  $X > \mu_d$ .  $C_1$  and  $C_2$  are the total capacitance on the floating gates, and  $T$  is the time the clock is low, typically half the clock period for a 50% duty cycle. We express the net shift in  $\mu$  for one clock cycle as  $\Delta\mu = \Delta V_1 P[X < \mu_d] - \Delta V_2 P[X > \mu_d]$ . Adaptation finishes when an equilibrium  $\Delta\mu = 0$  is reached

$$\Delta V_1 \Phi\left(\frac{\mu_d - \mu^*}{\sigma}\right) = \Delta V_2 \left[1 - \Phi\left(\frac{\mu_d - \mu^*}{\sigma}\right)\right]$$

where  $\Phi(x) = (1/\sqrt{2\pi}) \int_{-\infty}^x e^{-t^2/2} dt$  is the cdf of a Gaussian random variable with  $\mu = 0$  and  $\sigma^2 = 1$  and  $\mu^*$  the input offset after adaptation. Therefore, we express  $\mu^*$  as

$$\mu^* = \mu_d - \sigma \Phi^{-1}\left(\frac{\Delta V_2}{\Delta V_1 + \Delta V_2}\right) = \mu_d - \sigma \Phi^{-1}\left(\frac{1 - \rho}{2}\right) \quad (2)$$

where  $\rho = (\Delta V_1 - \Delta V_2)/(\Delta V_1 + \Delta V_2)$  is the injection mismatch ratio, the normalized difference in voltage change between the two floating nodes due to injection during one clock cycle. Note that this mismatch can result from either mismatch in injection current or from mismatch in floating node capacitance. We can see that the residual input offset is not a function of the device mismatch, but rather a function of both injection mismatch ratio  $\rho$  and the standard deviation  $\sigma$  of the input-referred noise. Fig. 5 shows the absolute value of the residual input offset  $|\mu_d - \mu^*|$ : (a) as a function of  $\rho$  for several values of  $\sigma$ , and (b) as a function of  $\sigma$  for several values of  $\rho$ .  $|\mu_d - \mu^*|$  increases rapidly when injection is extremely unbalanced. For up to 68% injection mismatch ( $|\rho| \leq 0.68$ ),  $|\mu_d - \mu^*|$  is bounded by the magnitude of  $\sigma$ . Therefore, even with severely imbalanced

injection currents we can obtain accurate calibration. Furthermore, we can improve the accuracy of calibration by increasing the gain  $A_V$  and therefore decreasing the input-referred noise  $\sigma_{V_i}^2 = \sigma_{V_o}^2/A_V^2$ , where  $\sigma_{V_i}^2$  is the input voltage noise variance and  $\sigma_{V_o}^2$  is the output voltage noise variance, as long as the output noise does not increase as much as the gain. For matched injection currents, we achieve zero offset ( $\mu^* = \mu_d$ ) regardless of  $\sigma$ .

During injection, the gate voltages are raised to a high programming common-mode voltage. During operation, the gate voltages are kept below an operating common-mode voltage limit to prevent injection. This difference in operating conditions during and after adaptation may introduce a small additional offset in the calibrated comparator. This imposes design constraints on the common-mode input voltages used for programming and for normal operation: ideally the common-mode voltages should be as close as possible for accurate calibration, but different enough to provide significant injection during programming with negligible injection during normal operation.

### C. Tradeoff Between Resolution and Speed

Since offset resulting from device mismatch can be canceled, the resolution of the AFGC is determined by the input-referred noise. For perfectly calibrated devices, the error introduced by this noise will be random and may be reduced by examining the comparator's outcome over many evaluation cycles. When the devices are not perfectly calibrated, the residual offset contributes an additional source of input-referred noise which is deterministic. Under realistic conditions, this deterministic noise is smaller than the random noise (see above). The relative magnitudes of the deterministic and random noise sources are determined by the injection mismatch ratio.

In the remainder of this section, we investigate the inherent tradeoff between speed and resolution that occurs for random noise in a single evaluation cycle. For simplicity, we consider only thermal noise. The total mean-squared current noise power across  $V_{o+}$  and  $V_{o-}$  is  $\bar{i}_T^2 = \sum_i \bar{i}_i^2 = 4kT(2/3)(g_{m1} + g_{m2} + g_{m3} + g_{m4}) \cdot B$  (in units of  $A^2$ ), where  $k$  is Boltzmann's constant,  $T$  the temperature in Kelvin, and  $B$  the noise-equivalent bandwidth (NEB). The input-referred voltage noise power equals  $\bar{v}_i^2 = g_{m12}^{-2} \bar{i}_T^2 \approx 8.4 \times 10^{-17} \cdot B$  (in units of  $V^2$ ), given a tail current of 100  $\mu A$ , a clock voltage of 3.3 V, a room temperature  $T = 300$  K, the device geometries and the process parameters. Next, we calculate NEB as  $B = (\pi/2) f_3 \text{ dB}$  [13] where  $f_3 \text{ dB} = ((g_{m34} + g_{m5})/2\pi C_L)$ . Using capacitance extracted from layout, we find that the RMS input noise is  $v_{i,RMS} = \sqrt{\bar{v}_i^2} = 320 \mu V$ . Under balanced operation with a fixed tail current,  $g_{m12}$  and  $g_{m34}$  are constant. Since  $g_{m34} + g_{m5}$  is a function of  $V_{clk}$ ,  $f_3 \text{ dB}$  and  $v_{i,RMS}$  also become functions of  $V_{clk}$ . As  $V_{clk}$  decreases,  $g_{m34} + g_{m5}$  and  $f_3 \text{ dB}$  decrease, and input noise is reduced. Fig. 6(a) shows the maximum clock frequency as a function of the clock voltage  $V_{clk}$ , obtained from the gate delay determined by simulation of an AFGC circuit extracted from layout. The gate delay is taken as the settling time between the clock transition and the convergence of the output voltages to the RMS noise level during reset. The settling time of evaluation is determined by the time required for divergence of the output voltages to within 10% of the power supply and is found to be 1 ns. This evaluation time is limited

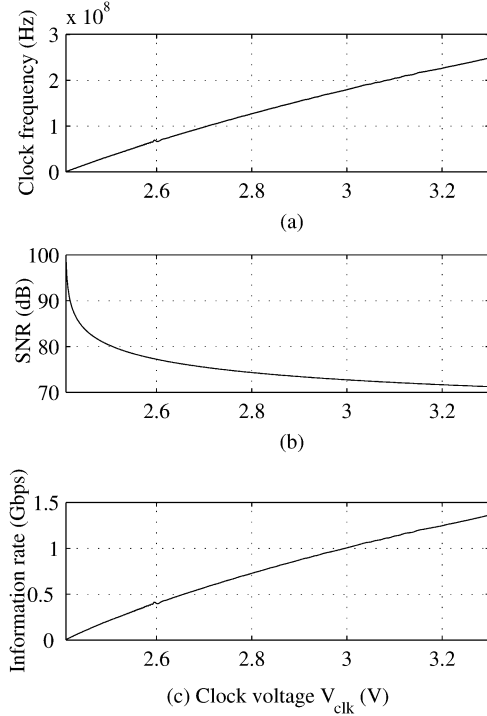


Fig. 6. Increasing  $V_{\text{clk}}$  increases speed, bandwidth, and noise, decreasing signal-to-noise ratio and increasing total capacity. (a) Maximum clock speed. (b) SNR. (c) Channel capacity as a function of the clock voltage, determined by simulation of an extracted AFGC circuit.

by the tail current and is less than the reset settling time for  $V_{\text{clk}} \leq 3.3$  V. Therefore the reset time dominates the gate delay and the speed depends on  $V_{\text{clk}}$ . Under the standard assumption that the input signal is a sinusoid with peak-to-peak voltage equal to the power supply (3.3 V), the signal to noise ratio is the ratio between signal power and the input-referred noise power. In Fig. 6(b) we plot the signal-to-noise ratio ( $\text{SNR} = 20 \log_{10}(1.65/\sqrt{2}/v_{i,RMS})$  dB) as a function of  $V_{\text{clk}}$ . Note that the speed increases with  $V_{\text{clk}}$ , but SNR decreases with  $V_{\text{clk}}$ . The channel capacity, or maximum number of bits per second for any signal distribution having a peak-to-peak voltage constraint, can be computed from the noise variance and the bandwidth as  $C = f \cdot \log_2(1 + (2/\pi e)(1.65^2/v_i^2))$  [14]. Fig. 6(c) plots the channel capacity  $C$  as a function of  $V_{\text{clk}}$ . Whereas increasing  $V_{\text{clk}}$  increases the operating speed, which tends to increase capacity, it also reduces gain, increases noise and reduces the accuracy of the comparison, which tends to decrease capacity. The net effect is an increase in the capacity as  $V_{\text{clk}}$  increases.  $C$  provides an upper bound of the information transmission rate of an analog-to-digital-converter (ADC) constructed using AFGCs with the conversion outcome determined in a single clock cycle.

#### D. Monte Carlo Simulation

In order to verify the performance of the AFGC using dynamic injection, we perform Monte Carlo simulation using HSPICE with the circuit netlist extracted from layout. We use the poly and poly-2 layers to form 216 fF capacitors at the input, coupling the input signals  $V_{i+}$  and  $V_{i-}$  to the floating gates  $V_{g+}$  and  $V_{g-}$ , respectively. We use the top layer poly-2 as the floating node rather than poly in order to minimize parasitic capacitances to ground. This floating node is connected

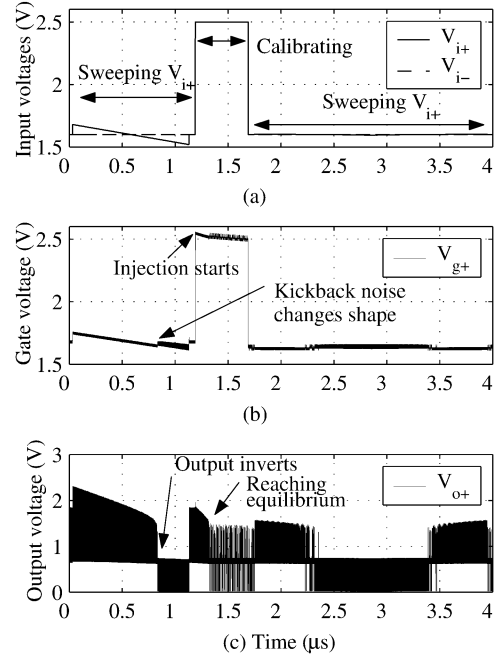


Fig. 7. Simulation traces depicting one calibration cycle in a series of Monte Carlo simulations, depicting: (a) input voltages  $V_{i+}$ ,  $V_{i-}$ ; (b) floating node output voltage  $V_{g+}$ ; and (c) output voltage  $V_{o+}$ .

to the gate of a pFET transistor via metal-1. The gate oxide capacitance is 40 fF, so we anticipate 17% reduction in the input voltage swing due to charge sharing. We use a 100  $\mu\text{A}$  tail current, a 50% duty cycle 340 MHz clock, and a “high” clock voltage  $V_{\text{clk}} = 3.3$  V. We augment the extracted netlist using the model from [11] to compute injection current (1). We increase the scale factor  $\alpha$  by  $10^7$  to accelerate injection and reduce simulation time. We use the Monte Carlo method to simulate process variation in the following parameters: poly gate length, diffusion width, pFET and nFET threshold voltages, and injection scale factor  $\alpha$  mismatch. Each process variation is specified as a Gaussian distribution with a given mean and standard deviation ( $\sigma$ ), and values for each transistor are chosen independently. We use  $\sigma_L = 0.6\%$  of minimum gate length 0.4  $\mu\text{m}$ ,  $\sigma_W = 0.012 \mu\text{m}$ ,  $\sigma_{V_{thN}} = \sigma_{V_{thP}} = 10$  mV and  $\sigma_\alpha = 20\%$ . We approximate device noise by adding 3 parallel sinusoidal current sources across the output nodes  $V_{o+}$  and  $V_{o-}$  with amplitude  $\sqrt{2}\sigma_n/\sqrt{3}$  and frequency 1 GHz,  $\pi^{-1}$  GHz and  $\pi^{-2}$  GHz, respectively, where  $\sigma_n$  is 0.27  $\mu\text{A}$ . This simple quasi-random model is sufficient for transient analysis because the magnitude of variations on the output nodes matches that expected for random thermal noise. Although the spectral density differs from that expected for random thermal noise, it is of limited importance for transient analysis.

Fig. 7 shows results from one trial of the Monte Carlo simulation. Fig. 7(a) shows the input voltages  $V_{i+}$  and  $V_{i-}$ , Fig. 7(b) shows one of the floating-gate voltages  $V_{g+}$  for clarity, and Fig. 7(c) shows an output voltage  $V_{o+}$ . First, we bias  $V_{i-}$  at 1.6 V and sweep the positive input  $V_{i+}$  to find the point where the output inverts. The input difference at this point is recorded as the input-referred offset before calibration ( $\Delta V_i$ ). The AFGC suffers kickback noise on the floating-gate voltages from the switching outputs  $V_{o+}$  and  $V_{o-}$ , as reflected in the floating-gate  $V_{g+}$  shown in Fig. 7(b). Note the correlation between the

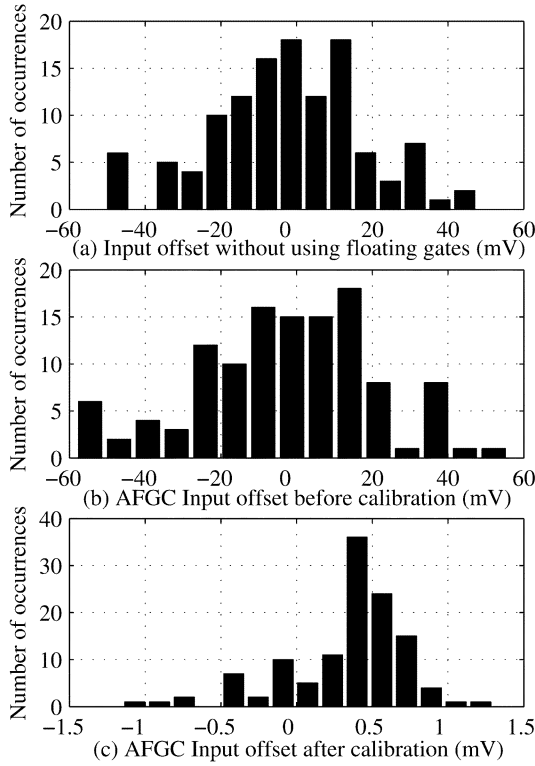


Fig. 8. Use of floating-gate transistors sacrifices gain at the input, but provides the ability to significantly reduce input offset. Histograms of input offset distribution determined through Monte Carlo simulations for (a) non-FG comparator and (b) AFGC before and (c) after calibration.

output states in Fig. 7(c) and the shape of the kickback noise in Fig. 7(b). Next, we raise both inputs to 2.5 V for 0.5  $\mu$ s to enable adaptation. During the calibration phase, the floating-gate voltage  $V_{g+}$  of Fig. 7(b) decreases. The output voltage shown in Fig. 7(c) alternates soon after calibration starts, indicating an equilibrium state. Finally, we sweep  $V_{i+}$  from high to low and then back up from low to high and record the differential input voltages at the two points where the output voltage switches. We then take the mean of the two to compensate circuit noise and obtain an estimate for the input referred offset after calibration ( $\Delta V_i'$ ). We perform 120 trials, each with Monte Carlo variables drawn from independent Gaussian distributions, and obtain the input offset distributions shown as histograms with 15 equally-spaced bins in Fig. 8. Fig. 8(a) is the simulated input offset distribution of a comparator of identical structure except that floating-gate transistors are replaced by normal pFET's. Fig. 8(b) is the simulated input offset distribution of the AFGC before calibration. Fig. 8(c) is the simulated input offset distribution of the AFGC after calibration. The standard deviation of  $\Delta V_i$  ( $\sigma_{\Delta V_i}$ ) in (a) is 20.4 mV, in (b) is 23 mV, and  $\sigma_{\Delta V_i'}$  in (c) is 413  $\mu$ V. The mean of  $\Delta V_i$  ( $\mu_{\Delta V_i}$ ) in (a) is -2.5 mV, in (b) is -2.9 mV, and  $\mu_{\Delta V_i'}$  in (c) is 332  $\mu$ V. Note that there is a small positive mean in Fig. 8(c) for the offsets after adaptation. It is likely that this offset results from residual injection during the sweeping of the input differential voltage, which is magnified in this simulation by a factor of  $10^7$  and is further enhanced by biasing the common-mode voltage  $V_{CM}$  at 1.6 V. This relatively high common-mode input voltage does not completely eliminate injection on the floating nodes and was chosen to reduce

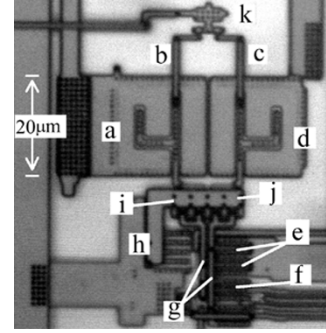


Fig. 9. Photomicrograph of a single AFGC. The floating-gate poly2 is sandwiched between the metal-poly enclosure labeled by (a) and (d), which are the input voltages  $V_{i+}$ ,  $V_{i-}$ , respectively. The floating gates are connected to the tunneling electrode and to the input transistors by metal1 labeled by (b) and (c).  $M_1$  and  $M_2$  are indicated by (i) and (j) respectively;  $M_3$  and  $M_4$  are indicated by (e), (f) indicates  $M_5$ , (g) indicates the two output nodes  $V_{o+}$ ,  $V_{o-}$ , (h) shows the tail current mirror and (k) shows the tunneling electrode.

the applied common-mode voltage change between adaptation and evaluation.

By using floating-gate transistors at the input, we sacrifice gain due to capacitive sharing, resulting in larger input standard deviation  $\sigma_{\Delta V_i}$ . However, the floating-gate transistors allow us to effectively reduce the input offset through adaptation, and under these simulation conditions we achieve a reduction of 55.7 (34.9 dB) in offset variance (a factor of 49.4 (33.9 dB) relative to the non-floating-gate comparator).

#### IV. EXPERIMENTAL RESULTS

The AFGC described in Section III has been fabricated in a commercially available 0.35- $\mu$ m CMOS technology with 2 poly layers and 3 metal layers. The layout has been implemented using scalable submicron rules [15], and one AFGC occupies an area of 52  $\mu$ m  $\times$  38.6  $\mu$ m (65  $\mu$ m  $\times$  38.6  $\mu$ m with the tunneling node) with  $\lambda = 0.2$   $\mu$ m. A photomicrograph of the fabricated circuit is shown in Fig. 9.

The circuit configuration used for testing the comparator is shown in Fig. 10. We supply the comparator with  $V_{CM}$  at the negative input  $V_{i-}$  and a differential voltage  $V_d$  between the differential inputs. The comparator depicted in Fig. 2 drives the output buffer of Fig. 10(a) to generate rail-to-rail signals  $0V \rightarrow 3.3$  V on  $V_{out+}$  and  $V_{out-}$ . A cascade of geometrically scaled inverters [16] in Fig. 10(b) deliver the signals to external pads with minimum delay. During reset  $V_{clk}$  is set "high" and both outputs of the comparator are high. During evaluation  $V_{clk}$  is set low and the outputs are determined by the comparison. We measure a low-pass filtered version  $V_A$  of the digital output voltage A, as shown in Fig. 10. We interpret this voltage to determine the probability that the output is logic high. We use a Keithley 236 to supply  $V_d$  in 100  $\mu$ V increments. For simplicity, we operate the clock at 100 kHz, and choose the time constant of the low-pass filter to be  $\tau = 2\pi RC = 0.01$  s, so that the clock frequency is much larger than  $\tau^{-1}$ , which is much larger than the measurement sampling frequency. Therefore, the output of the low-pass filter  $V_A$  approaches the mean value  $m$  of the outcome. As before, let  $X$  be the random variable representing the actual input offset, and suppose that the outcome is low ( $D_0 = 0$ ) when the differential input signal  $V_d$  is less than  $X$ , and high ( $D_1 = 1$ ) when  $V_d$  is greater than

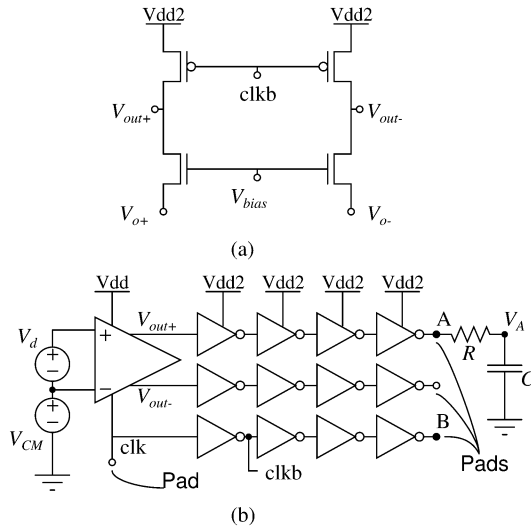


Fig. 10. Circuit configuration used for testing the voltage comparator. The comparator output drives an output buffer shown in (a) which generates rail-to-rail output signals  $V_{out+}$  and  $V_{out-}$ . (b) A cascade of geometrically scaled inverters delivers the signal offchip with minimal delay, and the externally filtered output voltage  $V_A$  is interpreted as the probability that the output is logic high.

$X$ . Then,  $m$  is equivalent to the cdf  $p_1 = P[X < V_d]$  since  $m = \sum p_i D_i = p_0 \cdot 0 + p_1 \cdot 1$ , where  $p_0 = P[X > V_d]$ . In practice, we measure  $V_A$  as a function of  $V_d$  (Fig. 4(a)), then translate the filtered output voltage into probability by shifting and scaling the voltage  $V_A$  so that it ranges from 0 to 1. We interpret the scaled reading as the Gaussian cdf, and extract  $\mu$  and  $\sigma$  from the data using a minimum squared-error curve-fitting procedure.

We measure a 5-ns propagation delay from the clock edge at node B to the output change at node A in Fig. 10(b) which corresponds to a sampling frequency of 100 MHz. Comparators with sampling frequencies  $\approx 1.3$  GHz have been reported in the same feature size [17]. The AFGC is current starved with a relatively small tail current, so it transitions slowly during evaluation. In future work, we expect to increase the speed of the floating-gate comparator by modifying the latch structure and output buffer.

#### A. Input Offset Distribution Among the Chips

We measured the offset for AFGC circuits on twelve different chips under three experimental conditions: as received from the foundry before any adaptation (“raw”), after 20 hours of UV irradiation, and after adaptation.  $V_{dd} = 4.5$  V for the AFGC, and  $V_{dd2} = 3.3$  V for the output buffers for all experimental conditions.  $V_{CM} = 1.6$  V, except during adaptation when  $V_{CM} = 2.5$  V (or higher).

Table I lists the mean and standard deviation of input offset voltage measured under the three experimental conditions described above for AFGCs from 12 different chips. For “raw” chips, the input offset has mean 45.35 mV and standard deviation of 73 mV. After 20 hours of UV-irradiation, the mean offset is reduced to 22.02 mV with a standard deviation of 6.37 mV. This suggests that a significant amount of random initial charge exists on the floating gate when the chip is fabricated and that UV irradiation allows this charge to dissipate. In effect, this initial charge constitutes an additional nondeterministic offset which is added to the AFGC during fabrication by implementing

TABLE I  
INPUT OFFSET STATISTICS

	mean	std
Raw	45.35mV	73mV
UV-irradiated	22.02mV	6.37mV
Programmed	-109 $\mu$ V	379 $\mu$ V

floating gates using two polysilicon layers. Rodriguez-Villegas and Barnes report a layout technique to minimize charge trapped on floating nodes [18], but we did not take advantage of this technique in the AFGC structure reported here. We then enable adaptation of the residual offset by briefly raising  $V_{CM}$  on the pFET input differential pair, then return to normal operation by reducing  $V_{CM}$ . After adaptation, the mean offset is  $-109 \mu\text{V}$  with a standard deviation  $\sigma_o = 379 \mu\text{V}$ . The maximum observed residual offset after adaptation is  $728 \mu\text{V}$ . Whereas UV irradiation allows charge imbalances to dissipate, the adaptation technique compensates for offsets due to device mismatch. We achieve a factor of 2 reduction in the input offset mean and an order of magnitude reduction in the standard deviation of the mean after the 12 raw AFGC chips were UV irradiated for 20 hours. We achieve a further two orders of magnitude reduction in input offset mean and one order of magnitude reduction in standard deviation of the mean after adaptation of the 12 UV-irradiated AFGC chips.

According to (2), residual offset after adaptation is a function of input-referred noise and injection mismatch. We infer the injection mismatch ratio ( $\rho$ ) from the measured input-referred noise ( $\sigma_n$ ) and residual offset. The injection is performed with  $V_{clk} = 3.3$  V, which results in input-referred noise  $\sigma_n \approx 1.025$  mV. We calculate the injection mismatch ratio  $\rho$  according to (2), and find that  $\rho$  has a mean value of 8.3% with standard deviation 28% and a maximum observed value of 52.2%. Therefore, the pFET injection currents exhibit significant variation among transistors, but this variation does not prevent adaptation from achieving a residual input offset less than the standard deviation of input-referred noise.

#### B. Dependence of Conversion Accuracy On Clock Voltage

Fig. 11 confirms that for lower  $V_{clk}$ , a finer resolution comparison can be made on the input signals. The voltage gain in the pFET differential pair is increased by lowering  $V_{clk}$ , so the input offset can be adjusted with higher resolution at the cost of longer time required for reset and for overall adaptation. If the clock voltage is too low ( $< 2.1$  V), reset will be incomplete, resulting in hysteresis in the comparison outcome and adaptation. We can avoid this problem by keeping the clock voltage above a level defined by the nFET threshold (0.7 V). Experimentally, we find that  $742 \mu\text{V}$  is a lower-limit for the input-referred noise  $\sigma_n$ . This exceeds the standard deviation of the input-referred offset (post calibration)  $\sigma_n > \sigma_o$ , which confirms that the input-referred noise dominates comparator resolution. Assuming that the input signal has a 3.3 V peak-to-peak swing,  $\sigma_n = 742 \mu\text{V}$  translates into 63.9 dB SNR or equivalently, 10 effective bits in a single comparison. By averaging over several calibration cycles we can reduce the contribution of circuit noise to reach the limiting resolution provided by the offset calibration procedure

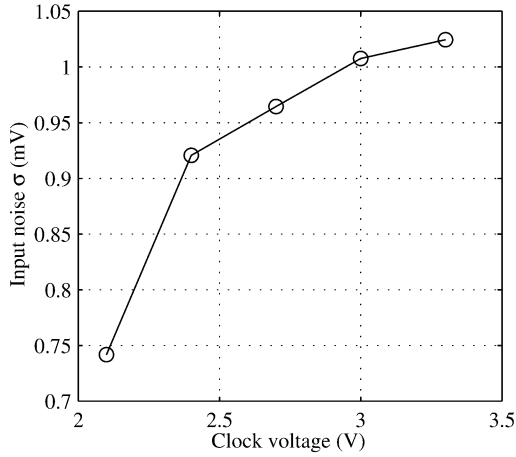


Fig. 11. Conversion accuracy depends on the clock voltage  $V_{\text{clk}}$ . Accuracy increases and input-referred noise decreases with higher circuit gain as  $V_{\text{clk}}$  is reduced.

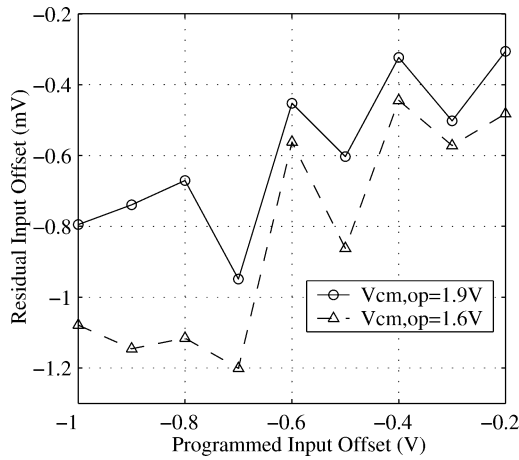


Fig. 12. Residual input offset voltages remain small over a wide range of programmed offset voltages.

( $\sigma_o = 379 \mu\text{V}$ ), which translates into 78.8 dB SNR or 13 effective bits. In this experiment, we used a bias current of  $40 \mu\text{A}$ ,  $V_{\text{CM}}$  of 1.2 V, Vdd of 4 V, and Vdd2 of 3.3 V, corresponding to AFGC power consumption of  $160 \mu\text{W}$ .

### C. Programming Input Offset in the $\pm 1\text{ V}$ Range

The AFGC can automatically cancel input offset, as shown above, or program a desired offset over a wide range of input values. This feature leads to compact and versatile implementations of flash data converters. Fig. 12 shows the residual input offset voltages after programming different offsets ranging from  $-1\text{ V}$  to  $+1\text{ V}$ . These experiments used  $V_{\text{CM}} = 2.5\text{ V}$  for adaptation. The residual input offset voltage is defined to be the programmed input offset minus the measured input offset. The solid trace shows the input offsets measured at  $V_{\text{CM}} = 1.9\text{ V}$ , and the dashed trace shows the input offsets when measured at  $V_{\text{CM}} = 1.6\text{ V}$ . From the figure we can see that larger shifts of  $V_{\text{CM}}$  from injection conditions result in larger offset errors during operation. This is caused by Early voltage mismatches on the pFET differential pair and channel length modulation on the pFET that sets the bias current for the p-type differential pair.

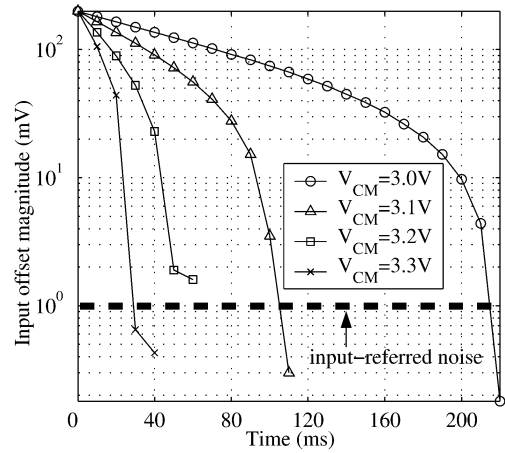


Fig. 13. Input offset decreases exponentially in time. Offset is initially 200 mV and decreases in time, with decay time constant decreasing with increasing  $V_{\text{CM}}$ .

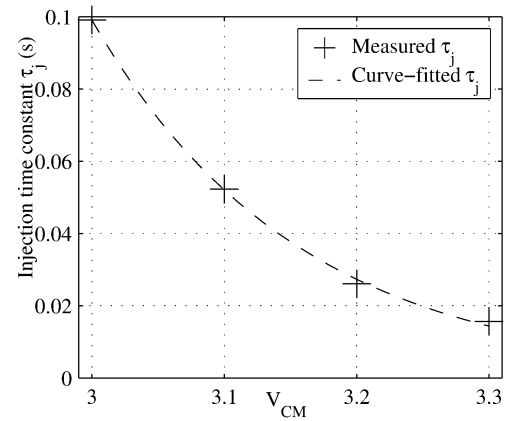


Fig. 14. Measured and fitted injection time constant  $\tau_j$  versus  $V_{\text{CM}}$ .

### D. Time Course of Offset Cancellation

Fig. 13 shows the time course of offset cancellation for AFGC circuits on four chips. The four traces show the absolute value of the input offset voltage under different input common-mode voltages during adaptation. We first program a 200 mV input offset on the gate, and then pulse  $V_{\text{CM}}$  to an appropriate injection voltage (between 3 V and 3.3 V) for 10 ms (1000 clock cycles) with  $V_d = 0\text{ V}$  and a clock frequency of 100 kHz. We measure input-referred offset voltage with  $V_{\text{CM}} = 1.9\text{ V}$  between each pulse. For higher programming  $V_{\text{CM}}$ , the residual input offset converges faster. For lower programming  $V_{\text{CM}}$ , convergence is slower. The time course is roughly exponential, as predicted by the injection model. It is important to note that after the residual offset converges it remains constant below  $\sigma_n$ , for all values of  $V_{\text{CM}}$ .

We assume that the input offset decays as  $\mu(t) = \mu_0 e^{-t/\tau_j}$ , from an initial value  $\mu_0 = 200\text{ mV}$  with injection time constant  $\tau_j$ . From the experimental data  $\mu(t)$  we can estimate  $\tau_j$ . The estimates are depicted as '+'s in Fig. 14 as a function of  $V_{\text{CM}}$ . The injection time constant ranges from 100 ms for  $V_{\text{CM}} = 3\text{ V}$  to 18 ms for  $V_{\text{CM}} = 3.3\text{ V}$ . The injection time constant decreases exponentially with  $V_{\text{CM}}$ , i.e.,  $\tau_j(V_{\text{CM}}) = \tau_{j0} e^{-k(V_{\text{CM}} - V_{thj})}$ , which is consistent with our simple model of injection. The time constant  $\tau_j$  is inversely proportional to the injection

current, which in turn is roughly exponential in gate-to-drain voltage. The gate-to-drain voltage scales with  $V_{CM}$ , and  $V_{thj}$  is the “injection threshold voltage”. We fit the data in Fig. 14 with a dashed line corresponding to  $\tau_{j0} = 1$  s,  $k = 6.43$  and  $V_{thj} = 2.64$  V. Experimentally we find injection starting around  $V_{CM} = 2.5$  V with adaptation occurring within seconds, confirming the accuracy of this simple exponential approximation.

### E. Robustness of Operation With Temperature and Time

Temperature and retention time studies of the AFGC are addressed in detail in [19]. Input offset is sensitive to temperature fluctuations. We measured the residual offset over a range of 20 °C after allowing the chip to equilibrate for 2 minutes. The coefficient of variation in input offset with temperature change for one device was  $+15 \mu\text{V}/^\circ\text{C}$ . Adaptation can be accomplished at any desired operating temperature by simply raising  $V_{CM}$  as described above, then returning  $V_{CM}$  to a suitable voltage for normal operation.

Relaxation of charge stored on the floating nodes after adaptation may cause drift of the input-referred offset over time. We have confirmed experimentally that the AFGC accurately retains offset for more than a month. We programmed initial offsets of 0 V and 100 mV, and periodically measured the residual input offset. Between each measurement, the chips were removed from the test fixture and stored on conductive foam. We performed the measurements using standard ESD protection without further precautions. For the chip programmed with 0 V, the offset drifted down by  $691 \mu\text{V}$  in the first 3 days, then stayed around  $-750 \mu\text{V}$  through the end of the experiment. For the chip programmed with 100 mV, the error stayed around  $-450 \mu\text{V}$  throughout the experiment. The initial drift is likely to be due to relaxation of the charge stored on the floating nodes or to further injection. Injection may continue to occur even when the inputs are biased at  $V_{CM} = 1.6$  V used for evaluation, as Vdd remains at 4.5 V (see simulation results and description in Section III-D).

### F. Overshoot in Static Injection

The results described in previous sections have been obtained using the dynamic injection method, with a running clock and update direction controlled by the outcome of each comparison during evaluation.

If instead of using a running clock, we supply a constant voltage at the clock terminal, the comparator becomes an amplifier with gain determined by  $V_{clk}$  and update direction controlled by the voltages at the outputs  $V_{o+}$  and  $V_{o-}$ . In this way, we observe the accuracy and time course of adaptation performed using the static injection method. Fig. 15 shows the time course of input-referred offset with a voltage of 3 V applied to the clock terminal. The setup is similar to the previous experiment (injection time course), but with a higher Vdd (5.3 V) and a longer  $V_{CM}$  pulsewidth (100 ms). As before, we program an initial input offset of 0.2 V, and record the input offset once every 100 ms during injection. As depicted in Fig. 15, the input offset voltage does not stop when the offset reaches 0 V at time 0.4 s, but rather continues to drop. This overshoot phenomenon exists because the currents in the two sides of the differential pair become unbalanced during programming. The injection current is

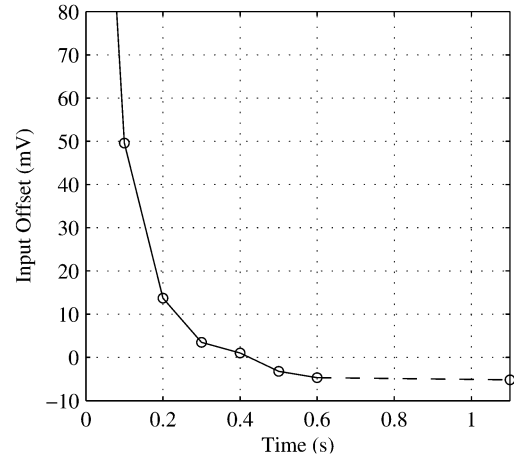


Fig. 15. Input offset for the static injection method with clock voltage held constantly high. Offset first decreases, then “overshoots” the desired point and settles at a nonzero offset voltage.

proportional to the channel current of the pFET transistor, and in order for correction to occur one injection current must be larger than the other. Injection continues until the two injection currents are equal, though the input offset is not.

## V. CONCLUSION

We have described a novel floating-gate comparator that can automatically and accurately cancel its input offset or allow programming of a specified offset. The AFGC uses pFET hot-electron injection in a negative feedback loop during calibration and programs a nonvolatile corrective charge on the floating gate. Residual input offset converges to the product of input-referred noise level and the inverse error function of the injection mismatch ratio; thus the residual offset is less than the input-referred noise standard deviation for an injection mismatch as large as 68%. Experiments show that adaptation consistently reduces residual offset to a fraction of input-referred noise for all observed values of injection mismatch. We experimentally demonstrate more than two orders of magnitude reduction in offset voltage: the mean offset is reduced by a factor of 416 relative to fabricated chips directly from the foundry and by a factor of 202 relative to UV-irradiated chips. The adaptation mechanism encompasses the entire comparator circuit and therefore the residual offset is independent of device mismatch. Experimental results confirm theoretical predictions for mismatch, injection and adaptation speed. In the presence of observed 8.3% injection mismatch, the AFGC robustly converges to within 728  $\mu\text{V}$  of the desired input offset (mean offset  $-109 \mu\text{V}$ , standard deviation 379  $\mu\text{V}$ ). Offset cancellation is achieved within milliseconds and the AFGC itself consumes  $\approx 300 \mu\text{W}$ .

In addition to canceling offset, the AFGC can accurately store an arbitrary input offset, a feature not readily available in other offset cancellation schemes. While the ability to program offsets is particularly amenable to compact implementations of flash data converters, the AFGC may be used in any data converter in which offset cancellation or programming is desired and two conditions can be satisfied: the desired differential input can be presented across the input terminals (i.e., the input terminals can be shorted for offset cancellation), and the common-mode input voltage can be raised to enable programming. Direct external

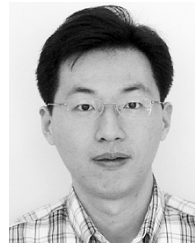
access to the terminals of each comparator is not necessary. The input common-mode shift required to enable adaptation can be accomplished using an auxiliary capacitor coupled into the floating nodes. We are currently designing system architectures which incorporate the AFGC into adaptive data converters that track changing environmental conditions and signal statistics.

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