

Current Mode Imager with Nonuniformity Correction and Edge Detection

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Abstract— We describe a current mode image plane processor for edge detection with adaptive nonuniformity correction. The correction is implemented at the pixel level using floating gate MOS transistors operating in the sub-threshold region. Edge detection is achieved through the convolution of the pixel array with programmable kernel matrices. Under uniform illumination, nonuniformity correction reduces the number of spurious edges detected, thus improving the quality and dynamic range of the image plane processors. A prototype array of 16×16 pixels with a pixel size of $44.8 \mu\text{m}$ by $48.3 \mu\text{m}$ and a fill factor of 21.25% has been designed in a commercially available $0.5 \mu\text{m}$ double poly, triple metal CMOS process.

I. INTRODUCTION

In CMOS imagers, image plane nonuniformities are created by mismatches in photodetectors and transistors. These mismatches give rise to fixed pattern noise (FPN) that degrades image quality and ultimately limits the resolution and sensitivity of the imaging system. The performance of any subsequent image processing will also be degraded by nonuniformity.

Various techniques for FPN correction have been suggested previously. The most commonly used technique employs correlated double sampling (CDS) [1]. Most methods for canceling FPN convert the photocurrent to a voltage regardless of whether the pixel is current mode or voltage mode, which induces further errors. An online technique for correcting image plane nonuniformity via floating gate adaptation was demonstrated by Cohen et al. [2]. This technique operates entirely in the current mode and uses hot electron injection to compensate for dark current nonuniformities and gain and offset mismatches.

Signal processing on an image can be integrated into the same circuitry that acquires the image through digital, mixed-signal, and analog circuit design techniques [4-7]. Digital implementations of image plane processors typically require high precision ADC, complex processor, and consequently high power consumption [4]. Image

plane processing has also been demonstrated using the mixed signal circuit design technique of CDS [5] and the analog circuit design technique of convolving an array of pixels with a programmable kernel matrix [7]. Here we report a design that enables powerful current mode signal processing with the ability to effectively remove nonuniformities due to offset and gain mismatch as well as dark current nonuniformities.

The remainder of this paper is organized as follows: Section II describes the method of nonuniformity correction. Section III describes the kernel computation for edge detection and its circuit implementation. Section IV describes the results achieved for edge detection without any adaptive correction versus that with adaptive gain correction. Section V summarizes the work.

II. NONUNIFORMITY CORRECTION

To improve the accuracy of edge detection, adaptation is implemented at the pixel level using floating gate MOS transistors.

A. Pixel Circuit Diagram

We use the exponential relationship between voltage and current in subthreshold operation of a MOS transistor to encode current gain as an exponential function of the voltage offset across a floating gate transistor. This relationship makes it possible to achieve current gain correction by adjusting voltage in the log domain. The gate voltage is controlled through impact-ionized hot electron injection onto the floating gate node and results in unidirectional change in transistor current gain. The injection mechanism has been extensively described in the literature [3]. Hot-carrier injection occurs in pFETs in the presence of strong lateral and vertical electric fields that increase the likelihood of generating high energy electrons and sweeping these hot electrons across the oxide barrier, respectively. For ordinary pFETs, it is relatively easy to achieve both conditions under normal operation.

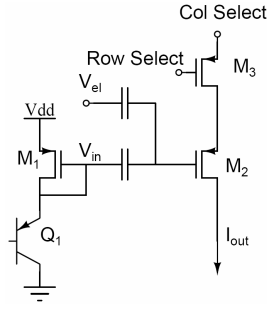


Figure 1. Pixel circuit diagram

The pixel circuit diagram shown in Fig. 1 is based on the adaptive floating gate pixel [2]. Phototransistor Q_1 converts photons into photocurrent. Transistor M_1 converts this photocurrent logarithmically into voltage, V_{in} . M_2 is a floating gate transistor with inputs V_{in} and the global control voltage V_{el} . When a constant current sink is applied at the pFET drain, hot-electron injection decreases the floating gate voltage until the transistor current matches the current bias: when the current sink is greater than the transistor current, the drain voltage is pulled low, when enables injection.

B. Adaptation Technique

Under uniform illumination, the pixel array is scanned to determine the maximum intensity and the intensity of every pixel is corrected to this value. If a pixel current is found to be lower than the maximum, then the drain of M_2 is connected to a low voltage V_{inj} and charge is injected onto the floating gate to increase the pixel output current. The correction is unidirectional because the injection mechanism can only transfer electrons onto the floating gate. In addition V_{el} can be used to tune the entire pixel array to a specific intensity range.

III. EDGE DETECTION

Gruev and Etienne-Cummings demonstrated a method for implementing kernel computations at the periphery of the pixel array [7], and our implementation of edge detection is based on their method.

A. Algorithm

A sub-array of 3×3 pixels is convolved with programmable kernel matrices to achieve a variety of kernel computations. The kernel matrix for horizontal edge detection is given by

$$\begin{bmatrix} -1 & 2 & -1 \\ -1 & 2 & -1 \\ -1 & 2 & -1 \end{bmatrix}$$

The convolution for the x-edge adjusts the center pixel according to the following equation.

$$I_{22new} = -I_{11} + 2I_{12} - I_{13} - I_{21} + 2I_{22} - I_{23} - I_{31} + 2I_{32} - I_{33} \quad (1)$$

To simplify the hardware the equation may be rearranged according to summation in the x and y direction of the convolution array to give

$$\begin{aligned} I_{X1} &= I_{11} + I_{13} & I_{Y1} &= I_{11} + I_{31} \\ I_{X2} &= I_{21} + I_{23} & I_{Y2} &= I_{12} + I_{32} & I_{ORG} &= I_{22} \\ I_{X3} &= I_{31} + I_{33} & I_{Y3} &= I_{13} + I_{33} \end{aligned} \quad (2)$$

Thus the expression for the horizontal edge reduces to

$$I_{22new} = -I_{X1} - I_{X2} - I_{X3} + 2I_{Y2} + 2I_{ORG} \quad (3)$$

This regrouping of terms in the linear combination achieves minimum pixel size and maximum number of independent computations in parallel. This method can be extended to two dimensional kernel computations including detection of angled edges and Gaussian smoothing.

B. Pixel and Kernel Computation Circuitry

Kernel computations are performed at the periphery of the imaging array. The convolution is achieved through a digitally controlled analog processor and results in a linear combination of pixel currents from the sub-array. The process of nonuniformity correction prior to the computation retains the simplicity of analog current mode processing while improving upon its accuracy.

The method of kernel computation necessitates the use of a modified pixel structure as shown in Fig 2a. In order to compute the X-edge kernel values, photocurrent (corrected or uncorrected) is mirrored thrice within each pixel to generate I_X , I_Y and I_{ORG} . These currents are then copied onto their respective bus lines and sent into the scaling circuit shown in Fig 2b, where they are scaled by the appropriate factors to implement the desired kernel. Digital control bits 1-5 control the magnitude of the scaling. In order to generate the terms in equation (3), the pixel currents of a 3×3 pixel matrix are sent through the scaling circuitry with the control bits correctly selected and are then summed up to generate the X-edge intensity.

This imager has two operating modes: correction and detection. In correction mode the imager is first illuminated with uniform intensity and the pixel array is scanned to determine the highest output current. All pixels are then sequentially corrected to this maximum intensity as described in section II. %Correction is defined as the fraction of the total number of pixels whose intensity has been corrected to the maximum intensity level in the uncorrected pixel array. In detection mode the imager is presented with an image which is then processed through the kernel computation circuitry to generate the X-edge intensities.

IV. SIMULATION RESULTS

A 16×3 array of pixels was simulated under conditions of uniform illumination. The method for simulation of the edge detection circuitry is shown in Fig 3. Initial FPN

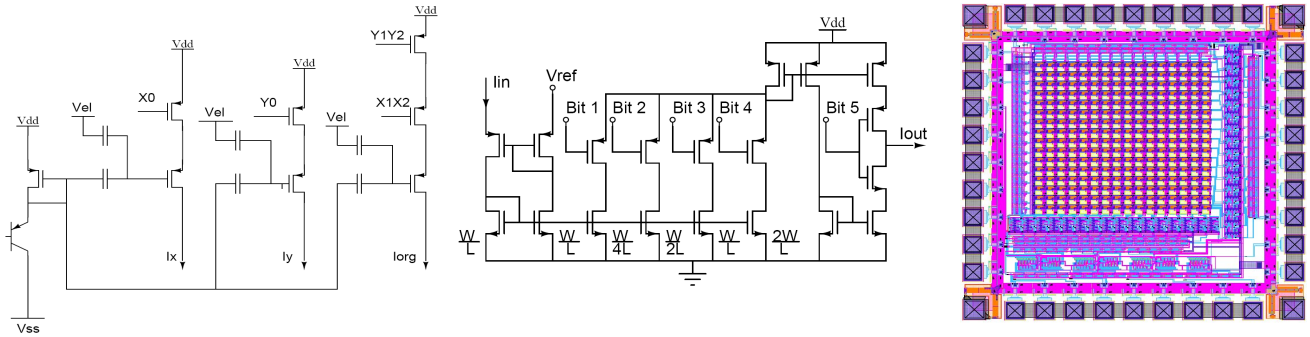


Figure 2. a) Modified pixel structure to allow for correction & edge detection. b) Scaling circuit portion of the kernel computation circuit c) Imager layout

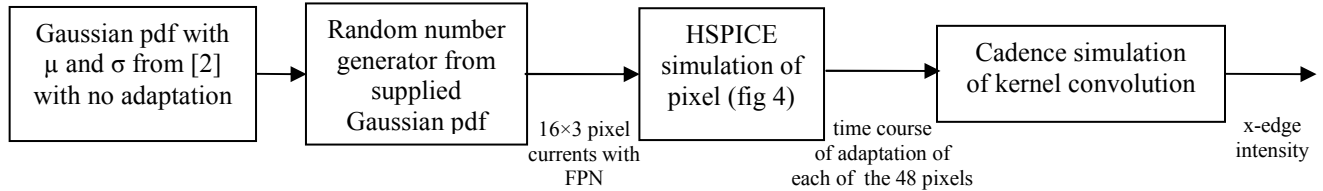


Figure 3. Method for simulation of edge detection.

offsets for each of 16×3 pixels were assigned according to a Gaussian probability density distribution with mean and standard deviation derived from experimental results in [2]. Hot electron injection was simulated using Hspice to determine the time required to complete nonuniformity correction for each pixel. To simulate current injection onto the floating gate, the injection model and simulation technique suggested in [3] was used. As correction progresses, the floating gate voltage of each pixel decreases due to charge injection and the corresponding pixel output current increases (Fig 4.). At different values of %correction, the current intensities of all the pixels in the array were determined. These current intensities were then used as inputs to the edge detection circuitry, which was simulated in Cadence

The x-edge intensity for a 14×1 row of pixels at these times during non-uniformity correction is shown in Fig 5. An edge intensity current of 50nA or higher is taken to be

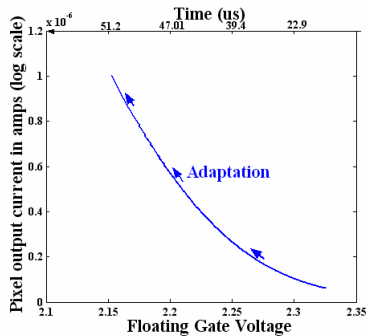


Figure 4. Output current of the floating gate transistor as a function of floating gate voltage

a spurious edge. The edge intensity for an uncorrected image is as high as 176nA and generates 8 spurious edges.

Both edge intensity and the number of spurious edges decrease as correction proceeds with only 3 spurious edges detected at 90% correction (Fig 6a). Fig 6b indicates that as correction proceeds, the mean intensity of the pixel array approaches the maximum intensity at 352nA. However, the pixel current with the lowest intensity in the array is corrected only by half (to 288nA) when 90% of the pixels are fully corrected. Thus, with the lowest intensity pixel present in column 13, high edge intensities are generated in columns 11-14 even with 90% correction. Under illumination, lowering the detection threshold in the corrected imager would enable us to detect weaker edges with greater accuracy than in the uncorrected imager. A prototype array of 16×16 pixels with a pixel size of $44.8 \mu\text{m}$ by $48.3 \mu\text{m}$ and a fill factor of 21.25% has been designed and fabricated in a commercially available 0.5um CMOS process and is currently being tested. Fig 2c shows a layout of the fabricated chip.

V. CONCLUSIONS

We report a current mode image plane processor for edge detection with adaptive non-uniformity correction integrated into each pixel. The correction is implemented using floating gate MOS transistors, and edge detection is achieved through the convolution of the pixel array with programmable kernel matrices. This design strategy exploits the computational efficiency of analog current mode processing, and combines it with a robust mechanism to correct for pixel nonuniformity. This technique has the potential to significantly improve the resolution and dynamic range of image plane processors.

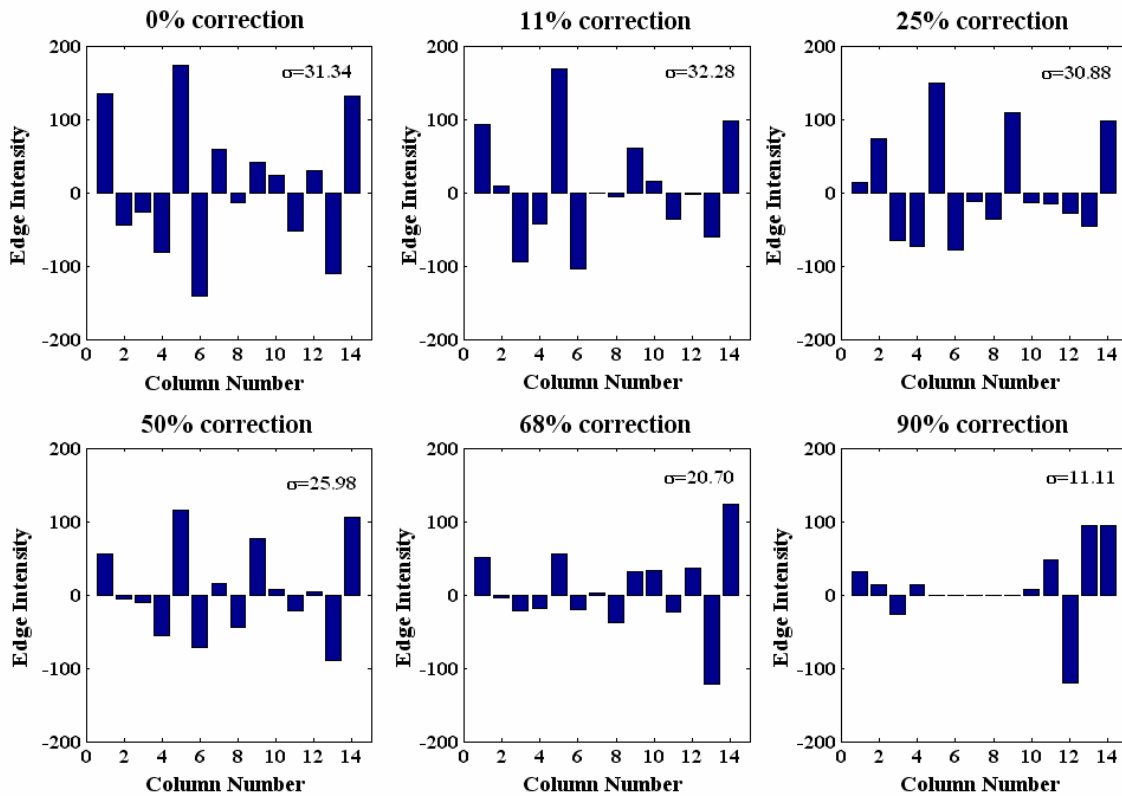


Figure 5. Edge intensity as a function of %correction. The standard deviation (σ_{edge}) of the edge intensity is indicated at each stage of correction.

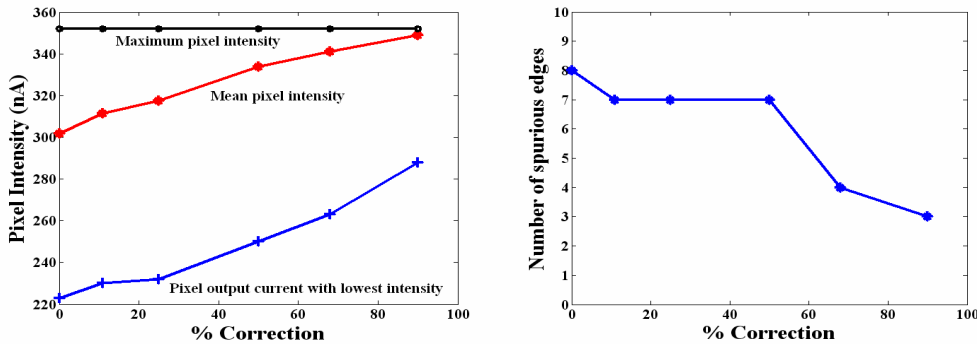


Figure 6. a) Pixel current intensity vs %correction b) Number of spurious edges vs %correction

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