



Differential Hot Electron Injection in an Adaptive Floating Gate Comparator

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Received September 24, 2004; Revised November 1, 2004; Accepted December 15, 2004

Abstract. We introduce *differential-mode hot electron injection* for adapting and storing analog nonvolatile signed state variables. This approach is compatible with modern digital CMOS technologies and is readily extended to novel circuit applications. We highlight advantages of the technique by applying it to the design of an adaptive floating gate comparator (AFGC). This is the first use of this technique for adaptation in a nonlinear circuit. The AFGC computes appropriate voltages for *locally* adapting the input floating gate nodes to cancel offsets. The technique is amenable to both local and nonlocal adaptation which allows greater design flexibility.

The AFGC has been fabricated in a commercially available $0.35\ \mu\text{m}$ CMOS process. We experimentally demonstrate more than two orders of magnitude reduction in offset voltage: the mean offset is reduced by 416X relative to chips direct from the foundry and by 202X relative to UV-irradiated chips. We consider both static and dynamic adaptation and demonstrate that the accuracy of dynamic offset cancellation is approximately two orders of magnitude better than static adaptation. In the presence of observed 8% injection mismatch, the AFGC robustly converges to within $728\ \mu\text{V}$ of the desired input offset (mean offset $-109\ \mu\text{V}$, standard deviation $379\ \mu\text{V}$). Adaptation occurs within milliseconds, with charge retention for more than one month, and variation of offset error with temperature of $-15\ \mu\text{V}/^\circ\text{C}$.

Key Words: differential, adaptation, analog-to-digital conversion, calibration, CMOS VLSI, comparator, floating gate, offset cancellation.

1. Introduction

We describe a design approach—differential hot electron injection—for adapting and storing signed state variables on floating gates and present a novel comparator circuit based on this approach. Hot electron injection is used to incrementally change the charge on floating gates in differential-mode circuit architectures. Although hot electron injection is a one-way process,

when used in combination with differential storage, it can represent signed state variables. Circuits that use this method of adaptation have been employed successfully in a number of *linear* circuit applications, including cancelling offsets at the inputs and outputs of differential amplifiers and tracking slowly varying signals for common mode feedback [1, 2]. We demonstrate the flexibility of the technique by extending it to a *nonlinear* dynamic logic circuit. We highlight the design of a novel adaptive floating gate comparator (AFGC), in which the technique provides a robust, compact and effective method for adapting and storing high resolution signed state variables. The AFGC is a clocked comparator that can be precalibrated or continuously updated with each clock cycle during dynamic operation.

We first discuss the technique of differential hot electron injection and then its application in a novel adaptive nonlinear circuit. Section 2 also describes the

Material in this paper was presented at the IEEE International Symposium on Circuits and Systems (ISCAS) in Vancouver BC, Canada, in May 2004 and appears in the Proceedings of ISCAS 2004. A more detailed description of the adaptive floating gate comparator (AFGC) has been accepted for publication in Transactions on Circuits and Systems I. This manuscript introduces the technique of weight storage and adaptation using “differential-mode” hot electron injection on floating gates and presents new experimental results on the AFGC’s analog weight retention as a function of time and operating temperature.

circuit architectures and physical mechanisms which enable storage and update of signed state variables via differential hot electron injection. In Section 3, we present the AFGC as an accurate and fast comparator that uses differential nonvolatile charge storage. We discuss two adaptation methods, static and dynamic, and analytically evaluate their effectiveness. We simulate input offset distributions of a comparator that does not have floating gate transistors and compare the resulting offset statistics with those of a comparator with floating gate differential input transistors before and after adaptation. In Section 4, we present detailed experimental results from the AFGC on adaptation accuracy, implications for A/D conversion accuracy, offset distribution before and after adaptation, and the time course of adaptation. We report measured statistical parameters for injection mismatch and the dependence of injection time constant on common-mode bias. Additional measurements demonstrate the robustness of the AFGC with respect to the retention time of stored weight values and with respect to changes in operating temperature. Measurements using both static and dynamic adaptation of the AFGC reveal that the accuracy of offset cancellation using the dynamic paradigm is approximately two orders of magnitude better than that achieved using the static paradigm.

2. Differential Injection for Storage and Adaptation

The technique of differential hot electron injection combines local differential nonvolatile storage together with appropriate control signals in order to update the local signed state variable. In practice the update is accomplished by injecting hot electrons onto one of the differential floating nodes connected to the gates of a differential pair.

Some existing schemes for floating gate adaptation use both hot electron injection and tunneling to achieve stable state variable adaptation [1, 3–5]. Tunneling requires high voltages during programming and operation; use of high voltages requires special high-voltage circuit design and layout considerations, and the high voltage supply must either be provided by an auxiliary power supply or generated on chip using DC-to-DC conversion techniques [6, 7]. In contrast, differential-mode adaptation uses the more readily integrated technique of hot electron injection for updating the state variables. Fowler-Nordheim tunneling is used only to

fix the initial values and common mode voltages of state variables; other mechanisms such as UV illumination or capacitive coupling of an auxiliary electrode can also be used for this purpose [8, 9].

2.1. Nonvolatile Local Storage

Local storage of analog state variables is used in many applications such as offset adaptation, parameter storage for neural networks or associative memories, and template storage for classifiers [3, 10–12]. While it is possible to store analog variables in volatile format on leaky capacitors [13, 14], this often limits architectures and applications to those employing continuous state variable updates. *Floating gates* are an enabling technology that provide a nonvolatile means for storing analog state variables as charge trapped on an electrical node surrounded on all sides by insulator. This *isolated* electrical node serves as the gate of a CMOS transistor that controls the current that flows through the channel of the device. Although it is feasible to implement nonvolatile floating gate storage in standard digital CMOS technology by implementing capacitances using MOS capacitors or metal-polysilicon capacitors, the circuits reported here use linear capacitors between layers of polysilicon. The technique of differential-mode injection does not require linear capacitors and is compatible with standard digital CMOS technology.

2.2. Adaptation of Local Nonvolatile Memory

The mechanism of hot electron injection has been extensively described in the literature [1, 15], and the injection feedback mechanisms for both nFET and pFET are discussed in detail in [16]. We briefly summarize the impact-ionized hot-electron injection mechanism for pFETs. For prevalent CMOS fabrication technologies, the efficiency of nFET hot electron injection is significantly reduced by lightly doped drain regions which coincide with the regions of highest electric field and reduce the lateral fields experienced by carriers. The techniques described in this paper may be applied using either nFET or pFET injection as appropriate in the CMOS technology of choice.

Minority holes traveling through the depletion region of a pMOS transistor's channel experience strong electric fields and acquire significant kinetic energy. Upon collision with the silicon lattice, these carriers can

undergo impact ionization and generate secondary carriers. The secondary electrons also experience strong electric fields; they can acquire sufficient energy to enter the oxide conduction band and may be collected at the floating node by a vertical electric field across the gate oxide. Two necessary conditions for hot electron injection in a pFET are: strong horizontal electric field or large $(V_s - V_d)$ and strong vertical electric field or large $(V_s - V_g)$. Minimum values for $(V_s - V_d)$ and $(V_s - V_g)$ that enable injection are technology-dependent parameters.

For simultaneous pFET injection and tunneling, a constant drain current configuration exhibits negative feedback from the drain voltage to the floating gate voltage, which drives the floating gate to a stable operating point. A large current sink at the drain node lowers the drain voltage and produces strong injection, which lowers the voltage at the floating node. This increases the current drive through the transistor and raises the drain voltage, which reduces injection. Lowering the floating node voltage increases the tunneling current, which in turn increases the voltage at the floating node. This process continues until the injection and tunneling currents balance, and the voltages at the drain and floating nodes equilibrate. This technique is used to cancel DC signals in the autozeroing floating gate amplifier (AFGA) [4]. Figure 1(a) is the configuration used in the autozeroing amplifier [4], and Fig. 1(b) is the *gate follower* configuration used in differential-mode injection. They are both constant current configurations where the current source is used in different locations; at the drain in Fig. 1 (a), and at the source in Fig. 1(b).

An accurate semi-empirical model in [17] suggests that an electron current I_{inj} is injected from the channel

onto the floating gate

$$I_{inj} = \alpha I_{source} \exp \left[-\frac{\beta}{(V_{gd} + \delta)^2} + \lambda(V_{gd} - V_{gs}) \right], \tag{1}$$

where $\alpha, \beta, \lambda, \delta$ are empirically fitted device parameters, I_{source} is the source current, and V_{gd} and V_{gs} are gate-to-drain and gate-to-source voltages. The current I_{inj} scales as an exponential function of gate-to-drain voltage V_{gd} . When V_{gd} increases, injection current I_{inj} also increases. The flow of electrons onto the floating gate decreases the gate voltage and reduces V_{gd} . In the constant current configuration of Fig. 1(b), the source voltage adjusts so that V_{gs} is approximately fixed. With V_{gs} fixed, injection proceeds to decrease the gate voltage until it reaches a value where the injection current stops. This negative feedback configuration causes the gate voltage to follow the drain voltage; hence the name *gate follower*. We use the *gate follower* configuration for adapting the floating gate nodes using differential injection, which couples control signals applied at the drains to the floating gate voltages to realize the appropriate signed adaptation of the state variable.

Since injecting electrons onto the floating gates of a differential pair can only lower the voltage of the floating nodes, injection always monotonically decreases the common mode voltage on the differential floating nodes. To ensure that the common mode voltage remains in a reasonable range for circuit operation, either tunneling [8], UV illumination, or an auxiliary electrode capacitively coupled to the floating gate nodes must be applied to establish the correct common mode operating voltage. We can employ injection and tunneling mechanisms to achieve the desired initial input common mode voltage. After setting the common mode voltage we perform adaptation using differential-mode injection. This two-step procedure sets a desired common mode voltage and a desired initial condition for the state variable at the same time.

The adaptation methods described above utilize charge transport across the thin gate oxides in modern CMOS technologies, which introduce concerns for the likelihood of oxide breakdown and device reliability. When gate and drain voltages are increased significantly beyond the maximum recommended power supply voltage for a process, the high vertical electric fields and high lateral electric fields can cause the gate oxide to deteriorate, permanently changing the threshold and leakage current of the affected FET devices.

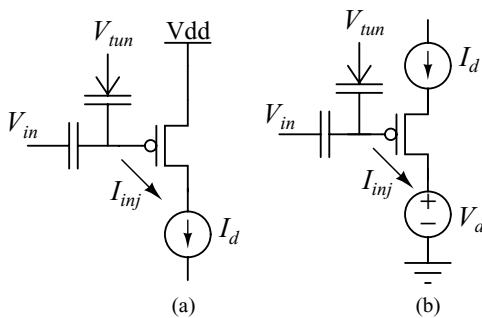


Fig. 1. Injection current exhibits negative feedback in the pFET constant current configuration in (a) the autozeroing amplifier [4] and (b) the *gate follower* used in differential-mode injection.

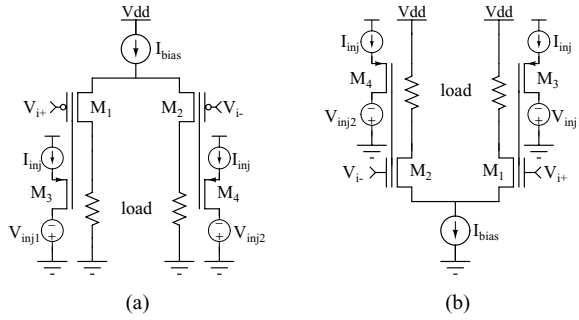


Fig. 2. Differential floating gate adaptation: (a) Circuit diagram of floating gate PMOS differential pair. (b) Circuit diagram of floating gate NMOS differential pair. Adaptation signals V_{inj1} and V_{inj2} control the update implemented by programming transistors M_3 and M_4 .

However, under the conditions employed for differential hot electron injection these concerns are allayed for several reasons. The time course of injection is typically short, injection current is self-limiting in the sense that it becomes weaker as adaptation proceeds, and the total injected charge is small. Further, the electric field strengths across the oxide are relatively low (<5 MV/cm) and decrease as adaptation proceeds. Finally, impact-ionized hot electron injection is intrinsically less likely to induce oxide damage as the charges transported across the gate oxide are electrons rather than holes, which have a lower energy barrier to enter the oxide conduction band [18], and the injection devices are pFETs rather than nFETs, which can tolerate higher charge injection [19].

2.3. Circuit Realizations

In differential-mode circuits, the input differential pair usually exhibits an offset due to threshold voltage variations or other fabrication mismatches. Output offsets observed for balanced inputs ($V_{i+} = V_{i-}$) can be mitigated by using floating gate transistors M_1 and M_2 in the input differential pair as depicted in Figs. 2(a) and (b) together with appropriate adaptation. In both circuits, voltage sources V_{inj1} and V_{inj2} control the sign of adaptation: when V_{inj1} is high the floating gate of M_1 is updated, and when V_{inj2} is high the floating gate of M_2 is updated. Programming transistors M_3 and M_4 differentially inject hot electrons onto the floating gates of transistors M_1 and M_2 respectively. Two equal current sources I_{inj} connected to the source terminals of M_3 and M_4 control the rate of adaptation. The charge

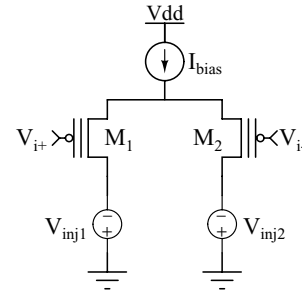


Fig. 3. Circuit diagram of floating gate pFET differential pair for the special case in which adaptation signals V_{inj1} and V_{inj2} are applied at the drains of M_1 and M_2 , eliminating the need for extra programming transistors.

update increment is determined by the initial charge on the floating node, the current I_{inj} , the programming voltage $V_{inj1,2}$, and the length of time that programming is enabled. Each of these injection circuits (M_3 , V_{inj1} , I_{inj} and M_4 , V_{inj2} , I_{inj}) are *gate followers* that control adaptation according to the values of the control variables V_{inj1} and V_{inj2} .

Figure 3 depicts a special case of Fig. 2(a) in which voltage sources V_{inj1} and V_{inj2} connect directly to the drains of M_1 and M_2 respectively, without the need for additional programming transistors. Together with their corresponding inputs V_{i+} and V_{i-} and tail current I_{bias} , this injection circuit controls the direction and rate of the adaptation. Transistors M_1 and M_2 are also *gate followers*.

The main distinction between the circuits of Figs. 2(a) and 3 is that Fig. 2(a) does not introduce constraints for the differential pair architecture, leaving the designer free to implement a wide variety of functions using appropriately selected loads. Figure 3, on the other hand, provides a somewhat more compact circuit, but introduces an architectural constraint that may not be suitable for all circuit applications.

The programming voltages $V_{inj1,2}$ may be computed *locally* within the differential circuit, or they may be computed *nonlocally* by another circuit or off-chip components. Adaptation itself is *local* when a device that stores a state variable also controls the update of that state variable. There are many examples of circuits in the literature that successfully use local control for adaptation [4, 14, 20]. The circuitry devoted to local adaptation is usually compact, with a high degree of parallelism, resulting in fast operation and transparency to the user. External biases may allow the user some flexibility in setting update rates.

In contrast, adaptation is *nonlocal* when a device that stores a state variable plays no role in the update of that state variable. Typically the nonlocal calculation of the adaptation control requires more complex circuitry (often off-chip), careful distribution of a “global” control signal much like the system clock used in synchronous digital logic, and higher power consumption [20–24].

The distinction between local and nonlocal control of adaptation is not always obvious. A new implementation of the AFGC separates the input differential stage from the output differential latching stage to achieve higher gain and therefore higher speed. In this case the adaptation control signals are local to the circuit itself, but computed separately from the devices in the circuit that hold the state variables [25].

In the compact AFGC implementation described in the following sections, we use the configuration of Fig. 3 and incorporate a regenerative element as the load to implement a latch which simultaneously produces the local voltage sources needed to control adaptation.

3. Adaptive Floating Gate Comparator (AFGC)

Comparators are nonlinear circuits that interface between analog and digital signals and are used in a wide variety of circuit applications, including analog-to-digital converters, memories, dynamic logic, and sense amplifiers. A modern comparator usually consists of a pre-amplifier, a decision circuit, and an output buffer. Mismatches due to process variation in the pre-amplifier and regenerative stages cause offset that directly affects resolution. A common and successful approach used to cancel offset is dynamic switching [26], which requires additional circuit components and multiple non-overlapping clocks. The AFGC requires one switch controlled by a single clock signal to adapt out the offset.

Since offset is a constant value for constant operating conditions, it is natural to store it using nonvolatile storage on a floating gate. Floating gate circuits have been used to cancel offsets in imagers [27], to trim current sources [5, 28, 29], and to autozero amplifiers [1, 4]. The ability to store desired nonzero offsets in comparators is a feature that is not readily available using existing offset cancellation techniques but is intrinsic to the voltage comparator we describe here.

Figure 4(a) shows the implementation of the AFGC. Floating gate pFET transistors M_1 and M_2 form the in-

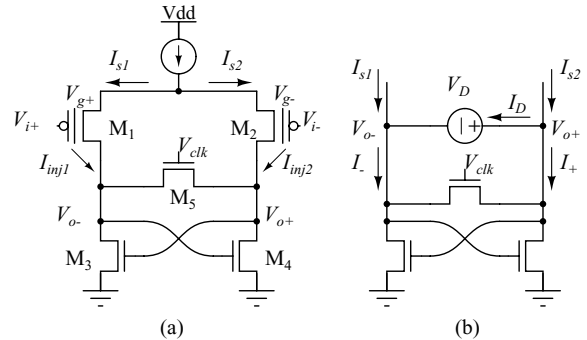


Fig. 4. Adaptive Floating Gate Comparator (AFGC): (a) Circuit diagram of the AFGC with pFET input floating gate differential pair, crosscoupled nFET regenerative elements, and reset switch. (b) Bias voltage on the reset switch determines conductance of the regenerative elements and overall gain during evaluation. Transconductance of the crosscoupled pair and switch is determined using HSPICE simulation of circuits extracted from layout.

put devices of a differential pair. Cross-coupled nFET transistors M_3 and M_4 form the regenerative elements of the comparator. When the clock signal V_{clk} is high, the nFET switch M_5 closes and resets the comparator. When the clock goes low, switch M_5 opens and the evaluation phase begins. With the power supply V_{dd} set to a normal operating voltage (3.3 Volts), there is insufficient energy to produce hot-electron injection from the channel onto the floating gates of M_1 and M_2 . As we increase voltage on the input terminals V_{i+} , V_{i-} and V_{dd} , the drain-to-channel voltages of M_1 and M_2 increase and the probability of hot electron injection onto the floating gates increases, thus injecting negative charge onto the floating gates. By accumulating negative charges on the floating gates, we form a negative feedback loop between the output and the input, achieving stable adaptation.

As discussed earlier in Section 2.2, differential hot electron injection as used in the AFGC is unlikely to cause significant gate oxide damage or introduce reliability concerns. We utilize pFET injection, where the gate voltage is within the power rails, and the source-to-drain voltage is just high enough for the channel to begin generating hot-electrons (which is close to V_{dd}); thus, we keep both vertical and lateral electric fields low, with maximal values 4.1 MV/cm and 5.6 MV/cm respectively. Further, the vertical field decreases as adaptation proceeds. The total time course of injection is typically short (≈ 100 ms), the corrective charge we inject across the oxide is small (20 fC for a 100 mV offset correction), and injection does not occur

constantly during operation. Thus, we keep the oxide damage to a minimum. In practice we have not observed such oxide degradation or related reliability problems in any of the devices we have tested, although we have not explicitly tested individual devices for breakdown characteristics. We measure charge retention times (see Section 4.7) of greater than a month, which indicates that the oxide integrity is maintained.

In the following sections we discuss two methods of adaptation, a static method and a dynamic method. The static method is simple and serves to illustrate the mechanism of adaptation, but its accuracy is limited in practice. The dynamic method overcomes the accuracy limitations of the simple static method and provides accuracy under 1 mV. We present simulations and measurements which demonstrate the efficacy of adaptation using the dynamic method.

3.1. Static Adaptation Method

The static method accomplishes adaptation during the reset phase of operation by applying a constant high voltage to the clock terminal. This constant voltage is chosen such that the comparator becomes an amplifier whose differential inputs $V_d = (V_{i+} - V_{i-})$ and outputs $(V_{o+} - V_{o-})$ are related by a high gain $A_V = \frac{V_{o+} - V_{o-}}{V_{i+} - V_{i-}} = cA_{fg}$. The constant c is the capacitance ratio C_{fg}/C_T , where C_{fg} is the capacitance between nodes V_{i+} and V_{g+} , and C_T is the total capacitance coupled to the floating node V_{g+} . The voltage gain A_{fg} from floating nodes V_{g+} and V_{g-} to the differential outputs is greater than the overall voltage gain A_V . The goal of offset cancellation is to balance the differential output $(V_{o+} - V_{o-})$ when the input difference is zero $(V_{i+} = V_{i-})$. Suppose that mismatch causes the outputs to be unbalanced $(V_{o+} > V_{o-})$ when the inputs are equal. When V_{i+} , V_{i-} and V_{dd} are raised sufficiently, injection occurs. Since the source-to-drain voltage of M_1 is greater than that of M_2 , the injection current I_{inj1} from the floating gate of M_1 will be greater than the injection current I_{inj2} at M_2 and the floating gate potential V_{g+} will decrease faster than V_{g-} . As a result, the differential current I_{s1} increases with a concomitant decrease in I_{s2} , causing the output voltage V_{o-} to rise and V_{o+} to fall. This feedback cycle drives the floating gate voltages V_{g+} and V_{g-} to values that compensate for the initial device mismatches.

The input-referred offset after adaptation depends on the voltage gain and mismatch of both device and in-

jection parameters. The voltage gain A_{fg} is the product of the input transconductance and the equivalent output resistance ($A_{fg} = g_{m12}R_{eq}$), where $R_{eq} = [r_{o12} \parallel r_{o34} \parallel (g_{m5} + g_{m34})^{-1}]$. We define conductance and resistance differentially, e.g., $g_{m12} = \partial(I_2 - I_1)/\partial(V_{g+} - V_{g-})$ and $r_{o12} = \partial(V_{o+} - V_{o-})/\partial(I_1 - I_2)$, where I_1 and I_2 represent the channel currents of M_1 and M_2 respectively. Note that for the positive feedback pair M_3 and M_4 , the conductance $g_{m34} < 0$. Suppose that there is an initial output offset $V_{o+} - V_{o-} = \Delta V_o > 0$ when $V_{i+} = V_{i-}$ and $V_{g+} = V_{g-}$ (i.e., the inputs are equal and there is no charge on the floating gate). Injection causes V_{g+} to drop by ΔV_{i+} and V_{g-} to drop by ΔV_{i-} , so when the injection currents equilibrate $I_{inj1} = I_{inj2}$ the differential output becomes $\Delta V'_o = V'_{o+} - V'_{o-} = (V_{o+} - V_{o-}) + A_{fg}(\Delta V_{i-} - \Delta V_{i+})$. Approximating injection current as $I_{inj} = \alpha I_{source} \exp[\frac{-\beta}{(V_{gd} + \delta)^2}]$ and assuming matched injection parameters α , β and δ and matched source currents $I_{source} = I_{s1} = I_{s2}$, we have:

$$\alpha I_{source} e^{\frac{-\beta}{(V_{g+} - \Delta V_{i+} - V'_{o-}) + \delta)^2}} = \alpha I_{source} e^{\frac{-\beta}{(V_{g-} - \Delta V_{i-} - V'_{o+}) + \delta)^2}}$$

$$(V'_{o+} - V'_{o-}) = (\Delta V_{i+} - \Delta V_{i-}) - (V_{g+} - V_{g-})$$

$$= (\Delta V_{i+} - \Delta V_{i-})$$

Therefore $\Delta V'_o = V'_{o+} - V'_{o-} = \Delta V_{i+} - \Delta V_{i-} = \Delta V_o - A_{fg}(\Delta V_{i+} - \Delta V_{i-})$, and $\Delta V_o = (\Delta V_{i+} - \Delta V_{i-})(1 + A_{fg})$, giving input referred offset after injection:

$$\Delta V'_i = \frac{\Delta V'_o}{cA_{fg}} = \frac{\Delta V_o}{cA_{fg}(A_{fg} + 1)}.$$

Consequently the input referred offset will be reduced by $(A_{fg} + 1)$ after adaptation. For high gain, we bias V_{clk} so that the conductance $g_{m5} + g_{m34}$ is small and positive. Note that this overall conductance $g_{m5} + g_{m34} = \frac{I_+ - I_-}{V_{o+} - V_{o-}}$ is the current difference $I_+ - I_-$ divided by the voltage difference $V_{o+} - V_{o-}$. We find this operating point from HSPICE simulation of a circuit extracted from layout using the configuration shown in Fig. 4(b). We set equal currents in the two sides of the differential pair ($I_{s1} = I_{s2}$) by applying equal gate voltages, and then introduce an offset voltage source V_D between V_{o+} and V_{o-} . We plot the current difference $-2I_D = I_+ - I_-$ as a function of the voltage difference $V_{o+} - V_{o-}$ in Fig. 5. The conductance $g_{m5} + g_{m34}$ depends on V_{clk} and can be found from the slope of the curves. Negative $g_{m5} + g_{m34}$ causes positive feedback during reset and results in hysteresis in the circuit

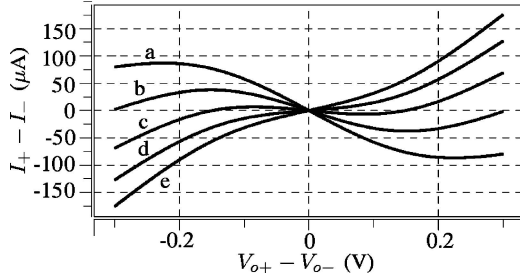


Fig. 5. Bias voltage V_{clk} controls the conductance of the switch and regenerative crosscoupled pair. Simulated current-voltage relationship for the circuit of Fig. 4(b) for V_{clk} from (a) 1.4 V to (e) 3 V in 0.4 V steps.

behavior. Negative $g_{m5} + g_{m34}$ occurs for low clock voltages ($V_{\text{clk}} \leq 2.2$ V, e.g., traces a,b and c). In order to maximize the gain A_{fg} and avoid hysteresis, V_{clk} is selected so that $g_{m5} + g_{m34}$ is positive ($V_{\text{clk}} = 2.6$ V in trace d of Fig. 5).

While the method of static adaptation described above may be used successfully to decrease offsets, both simulation and experiment (see Fig. 16) demonstrate the phenomenon of “overshoot”. We show that the ability to accurately cancel offsets is limited in practice when using the static adaptation method and explain the resulting overshoot in detail in Section 4.5 along with experimental results.

3.2. Dynamic Adaptation Method

The dynamic method overcomes the overshoot problem observed using static adaptation. Dynamic adaptation achieves injection during the evaluation phase when the clock signal V_{clk} is low, with adaptation achieved over many evaluation cycles. Whereas the accuracy of static adaptation is equal to the tolerance for a single increment, dynamic adaptation can achieve better accuracy with relaxed tolerance since error in one adaptation increment can be compensated in subsequent cycles. By injecting with a running clock, we use the outcome of each comparison to correct offset during the corresponding evaluation cycle. Thus the feedback loop encompasses all mismatch and offset within the circuit, and accurate offset cancellation can be achieved. We bias the common mode input voltage $V_{\text{CM}} = (V_{i+} + V_{i-})/2$ so that the drain-to-channel voltage is insufficient for injection during the reset phase of the clock cycle, but sufficient to produce injection during the evaluation phase when one of the outputs V_{o+} and V_{o-} is close to ground. From a simulation model

[17] and our own experimental results, injection begins when drain-to-channel voltage exceeds 3 V. For a pFET threshold of 1 V, we bias V_{CM} above 2 V. During reset both outputs are clamped at approximately the threshold voltage of an nFET $V_{o+} \approx V_{o-} \approx 0.7$ V, so we set the desired V_{CM} between 2 V and 2.7 V. For V_{CM} higher than 2.7 V, injection initially occurs during both reset and evaluation, but quickly reduces the common mode voltage of the floating nodes to 2.7 V, after which the circuit enters the desired operating range. Suppose that the initial mismatch causes the outputs to be unbalanced $V_{o+} > V_{o-}$ when inputs are equal. When the comparator latches, V_{o-} is pulled to ground, injecting a small charge Q_{inj} on the gate V_{g+} . The charge accumulates on gate V_{g+} for each clock cycle until the gate voltage is low enough that the outcome reverses ($V_{o+} < V_{o-}$). Thereafter, the outcome alternates for each cycle and causes injection on alternating sides of the p-differential pair. Adaptation proceeds until the common mode voltage on the floating gates is sufficiently low to prevent injection, or until injection is stopped by external reduction of the input common mode voltage. Adaptation is controlled by the outcome of the comparison and the offset can be tuned accurately.

In practice, any comparator has a limited conversion accuracy that can be defined by the variance of the input-referred noise. Ambiguity exists near the switching point where the outcome is uncertain. This uncertainty is caused by flicker noise and thermal noise generated by the MOSFETs within the circuit. The probability that the outcome is correct depends on how far the input is from the switching point. Empirically we find that this distribution is Gaussian, so we characterize the distribution with the mean and standard deviation obtained from the measured data. Figure 6(a) plots the measured comparison outcome as a function of the differential input voltage $V_d = V_{i+} - V_{i-}$ with an empirically fitted error function. This outcome is determined by observing the actual outcome through a low pass filter (see Fig. 10(b)) and detailed description in Section 4), and can be interpreted as the cumulative distribution function (cdf) of the actual outcome after normalization. Figure 6(b) shows the probability density function (pdf) corresponding to the fitted cdf with mean $\mu = -25.9$ mV and standard deviation $\sigma = 1.1$ mV.

Let X be a random variable representing the actual input offset having a nonzero mean μ and variance σ^2 . Then the cdf from Fig. 6(a) corresponds to $P[X < V_d]$. The goal of adaptation is for μ to approach a desired

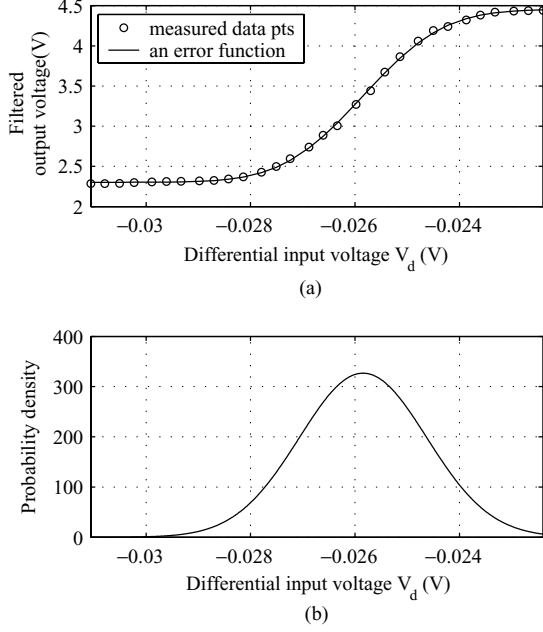


Fig. 6. Circuit noise causes uncertainty in the outcome of the comparison: (a) a typical input offset distribution, showing measured voltage distribution and empirically fitted error function, and (b) corresponding empirical Gaussian probability density function.

offset μ_d . For dynamic adaptation, during each clock cycle μ increases by $\Delta V_1 = C_1^{-1} \int_T I_{inj1} dt \approx Q_{inj1}/C_1$ for $X < \mu_d$, and decreases by $\Delta V_2 \approx Q_{inj2}/C_2$ for $X > \mu_d$. C_1 and C_2 are the total capacitances on the floating gates, and T is the time the clock is low, half the clock period for a clock signal with 50% duty cycle. We express the net shift in μ for one clock cycle as $\Delta\mu = \Delta V_1 P[X < \mu_d] - \Delta V_2 P[X > \mu_d]$. The adaptation finishes when an equilibrium $\Delta\mu = 0$ is reached,

$$\Delta V_1 \Phi\left(\frac{\mu_d - \mu^*}{\sigma}\right) = \Delta V_2 \left[1 - \Phi\left(\frac{\mu_d - \mu^*}{\sigma}\right)\right],$$

where $\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^x e^{-t^2/2} dt$ is the cdf of a Gaussian random variable with $\mu = 0$ and $\sigma^2 = 1$ and μ^* the residual input offset after adaptation. Therefore, we express μ^* as

$$\begin{aligned} \mu^* &= \mu_d - \sigma \Phi^{-1}\left(\frac{\Delta V_2}{\Delta V_1 + \Delta V_2}\right) \\ &= \mu_d - \sigma \Phi^{-1}\left(\frac{1 - \rho}{2}\right), \end{aligned} \quad (2)$$

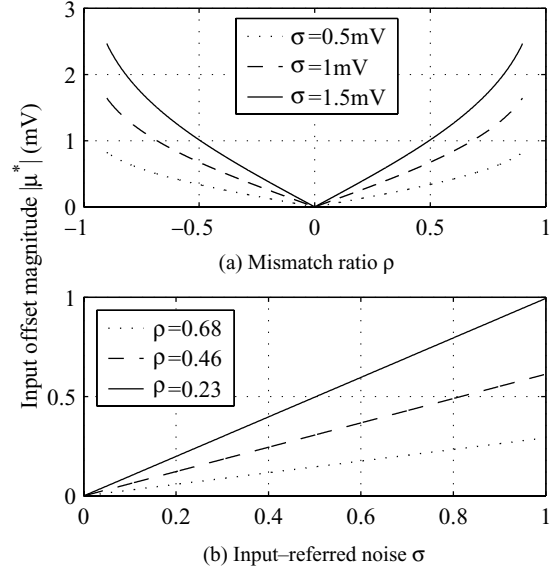


Fig. 7. Absolute value of the input offset $|\mu^*|$ after adaptation: (a) as a function of ρ for several values of σ , and (b) as a function of σ for several values of ρ .

where $\rho = (\Delta V_1 - \Delta V_2)/(\Delta V_1 + \Delta V_2)$ is the injection mismatch ratio, the normalized difference in voltage change due to injection in one clock cycle between the two floating nodes. Thus the residual input offset is a function of both injection mismatch ratio ρ and the standard deviation σ of the input-referred noise and is independent of device mismatch. Figure 7 shows the absolute value of the residual input offset $|\mu^*|$: (a) as a function of ρ for several values of σ , and (b) as a function of σ for several values of ρ . $|\mu^*|$ increases rapidly when injection is extremely unbalanced. For up to 68% injection mismatch ($|\rho| \leq 0.68$), $|\mu^*|$ is bounded by the magnitude of σ . Therefore, even with severely unbalanced injection currents we can obtain accurate adaptation. Furthermore, we can improve the accuracy of adaptation by increasing the gain and decreasing the input-referred noise. For matched injection currents, we achieve zero offset ($\mu^* = 0$) regardless of σ . In Section 4.1 we report experimental results for the input offset and input-referred noise, which allow us to estimate the injection mismatch ratio ρ empirically.

3.3. Monte Carlo Simulation

In order to verify the performance of the AFGC using dynamic injection, we perform Monte Carlo simulation

using HSPICE with the circuit netlist extracted from layout. We use the poly and poly-2 layers to form 206 fF capacitors at the input, coupling the input signals V_{i+} and V_{i-} to the floating gates V_{g+} and V_{g-} , respectively. We use the top layer poly-2 as the floating node rather than poly in order to minimize parasitic capacitances to ground. This floating node is connected to the gate of a pFET transistor via metal-1. The gate oxide capacitance is 40 fF, so we anticipate 17% reduction in the input voltage swing due to charge sharing. We use a $100 \mu\text{A}$ bias current and a 50% duty cycle 340 MHz clock. We augment the extracted netlist using the injection model from [17] that computes injection current (1). We increase the scale factor α by 10^7 to accelerate injection and decrease simulation time. We use the Monte Carlo method to simulate process variation in the following parameters: poly gate length, diffusion width, pFET and nFET threshold voltages, and injection scale factor α mismatch. Each process variation is specified as a Gaussian distribution with a given mean and standard deviation (σ), and values for each transistor are chosen independently. We use $\sigma_L = 0.6\%$ of minimum gate length $0.4 \mu\text{m}$, $\sigma_W = 0.012 \mu\text{m}$, $\sigma_{V_{thN}} = \sigma_{V_{thP}} = 10 \text{ mV}$ and $\sigma_\alpha = 20\%$. We approximate thermal device noise by adding 3 parallel sinusoidal current sources across the output nodes V_{o+} and V_{o-} with amplitude $\sqrt{2}\sigma_n/\sqrt{3}$ and frequency 1 GHz, π^{-1} GHz and π^{-2} GHz, respectively. σ_n is $0.27 \mu\text{A}$ for a V_{clk} of 3.3 V. Figure 8(a) shows the input voltages V_{i+} and V_{i-} , Fig. 8(b) shows one of the floating gate voltages V_{g+} , and Fig. 8(c) shows the output voltage V_{o+} . The AFGC suffers kickback noise on the floating gate voltages from the switching outputs V_{o+} and V_{o-} , as reflected in the floating gate V_{g+} shown in Fig. 8(b). Note the correlation between the output states in Fig. 8(c) and the shape of the kickback noise in Fig. 8(b). First, we bias V_{i-} at 1.6 V and sweep the positive input V_{i+} to find the point where the output inverts. The input difference at this point is recorded as the input referred offset before adaptation (ΔV_i). Next, we raise both inputs to 2.5 V for $0.5 \mu\text{s}$, enabling injection. As shown, the floating gate voltage V_{g+} decreases during injection. The output alternates soon after injection starts, indicating an equilibrium state. Finally, we sweep V_{i+} upward and downward and record the differential input voltages at the two points the output voltage switches. We estimate the input-referred offset after adaptation ($\Delta V_i'$) as the mean of the two values to compensate for circuit noise. We perform 120 trials, each with Monte Carlo variables drawn from independent

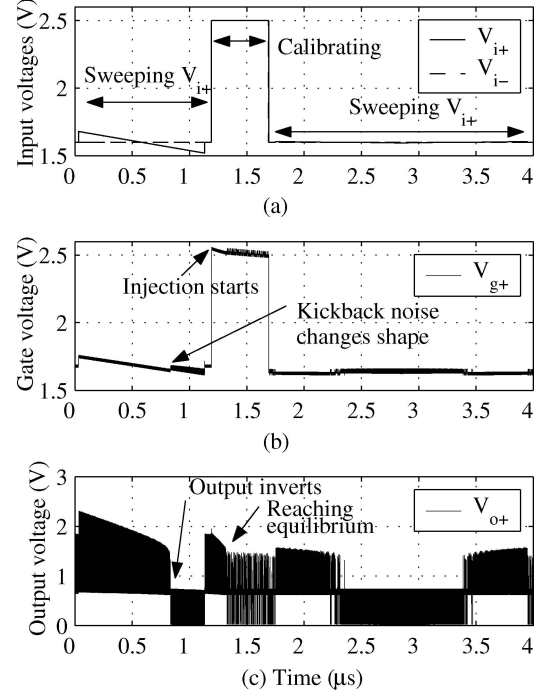


Fig. 8. Simulation traces depicting one adaptation cycle in a series of Monte Carlo simulations, depicting (a) inputs voltages V_{i+} , V_{i-} ; (b) floating node voltage V_{g+} ; and (c) output voltage V_{o+} .

Gaussian distributions, and obtain the input offset distributions shown as histograms with 15 equally-spaced bins in Fig. 9. Figure 9(a) is the input offset distribution of a comparator of identical structure except that floating gate transistors are replaced by normal pFETs. Figure 9(b) is the input offset distribution of the AFGC before adaptation. Figure 9(c) is the input offset distribution of the AFGC after adaptation. The standard deviation of ΔV_i ($\sigma_{\Delta V_i}$) in (a) is 20.4 mV, in (b) 23 mV, and $\sigma_{\Delta V_i'}$ in (c) is $413 \mu\text{V}$. By using floating gate transistors at the input, we sacrifice gain due to capacitive sharing, resulting in larger input deviation $\sigma_{\Delta V_i}$. However, the floating gate transistors allow us to effectively reduce the input offset, and under these simulation conditions we achieve a factor of 55.7 (35 dB) reduction in offset variance (a factor of 49.4 relative to the non-FG comparator).

4. Experimental Results

The circuit configuration used for testing the comparator is shown in Fig. 10. We bias the comparator with

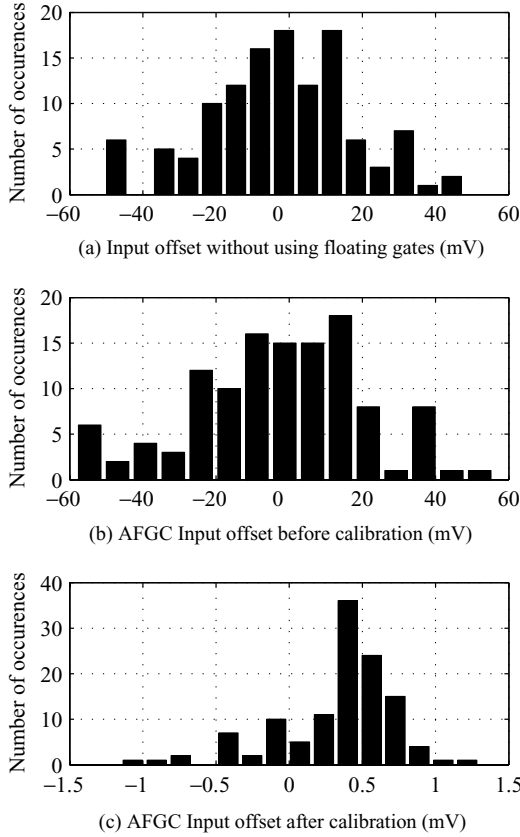


Fig. 9. The use of floating gate transistors sacrifices gain at the input, but provides the ability to significantly reduce input offset. Histograms of input offset distribution determined through Monte Carlo simulations for (a) non-FG comparator and (b) AFGC before and (b) after adaptation.

V_{CM} at the negative input V_{i-} and apply a differential voltage V_d between the differential inputs. The comparator depicted in Fig. 4 drives the output buffer of Fig. 10(a) to generate rail-to-rail signals on V_{out+} and V_{out-} . A cascade of inverters that are geometrically scaled [30] in Fig. 10(b) deliver the signals to external pads with minimum delay. During reset ($V_{clk} =$ high) both outputs of the comparator are high, and during evaluation the output is determined by the comparison. We measure a low pass filtered version V_A of the digital output voltage A, as shown in Fig. 10. We interpret this voltage to determine the probability that the output is logic high. We use a Keithley 236 to supply V_d in 100 μ V increments. For simplicity, we operate the clock at 100 kHz, and choose the time constant of the low pass filter to be $\tau = 2\pi RC = 0.01$ s, so that the clock frequency is much larger than τ^{-1} ,

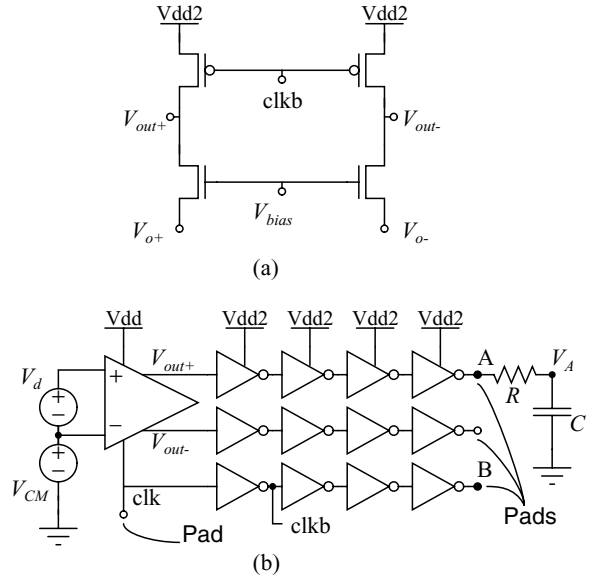


Fig. 10. Circuit configuration used for testing the voltage comparator. (a) The output comparator drives an output buffer which generates rail-to-rail output signals V_{out+} and V_{out-} . (b) A cascade of geometrically scaled inverters delivers the signal offchip with minimal delay, and the externally filtered output voltage is interpreted as the probability that the output is logic high.

which is much larger than the measurement sampling frequency. Therefore, the output of the low pass filter V_A approaches the mean value m of the outcome. As before, let X be the random variable representing the actual input offset, and suppose that the outcome is low ($D_0 = 0$) when the differential input signal V_d is less than X , and high ($D_1 = 1$) when V_d is greater than X . Then m is a scaled and shifted version of the cdf $p_1 = P[X < V_d]$ since $m = \sum p_i D_i = p_0 \cdot 0 + p_1 \cdot 1$, where $p_0 = P[X > V_d]$. In practice, we measure V_A as a function of V_d (Fig. 6(a)), then normalize the filtered output voltage by shifting and scaling in the Y-direction so that it ranges from 0 to 1. We interpret the scaled reading as the Gaussian cdf, and extract μ and σ from the data using a minimum squared-error curve-fitting procedure.

We measure a 5 ns propagation delay from clock edge (node B in Fig. 10(b)) to output change (node A in Fig. 10(b)) which corresponds to a sampling frequency of 100 MHz. Comparators with sampling frequencies ≈ 1.3 GHz have been reported in the same feature size [31]. The AFGC is current-starved with a relatively small tail-current, so it transitions slowly during evaluation. A new implementation of the AFGC

separates the input stages from the latch and introduces a modified output buffer to increase the speed [25].

4.1. Input Offset Distribution

We set V_{dd} to 4.5 V to allow injection and V_{dd2} to 3.3 V for the output buffers. We raise V_{CM} to 2.5 V (or higher) for programming, as demonstrated in the following experiments. We measure the offset for AFGC circuits on twelve different chips before any programming, after UV erasure, and after programming. For unprogrammed chips, the input offset has mean 45.35 mV and standard deviation of 73 mV. After 20 hours of UV erasure, the mean offset is reduced to 22.02 mV with a standard deviation of 6.37 mV. This means that a significant amount of random initial charge exists on the floating gate when the chip is fabricated. We then cancel the offset by initiating injection on the p -type differential pair. After programming, the mean offset is $-109 \mu\text{V}$ with a standard deviation of $\sigma_o = 379 \mu\text{V}$. The maximum observed residual offset after adaptation was $728 \mu\text{V}$. These results demonstrate more than two orders of magnitude reduction in offset voltage: relative to fabricated chips directly from the foundry, the mean is reduced by a factor of 416 and the variance by a factor of 193; relative to UV-irradiated chips, the mean is reduced by a factor of 202 and the variance by a factor of 17. Figure 11 shows the average offset before adaptation, after UV erasure, and after adaptation.

We infer the injection mismatch ratio (ρ) from the measured input-referred noise (σ_n) and residual offset. The injection is performed with $V_{clk} = 3.3 \text{ V}$, which results in input-referred noise $\sigma_n \approx 1.025 \text{ mV}$. We

calculate the injection mismatch ratio ρ according to Eq. (2), and find that it has a mean value of 8.3% with standard deviation 28% and maximum observed value of 52.2%. Therefore, the pFET injection currents exhibit non-negligible variation among transistors.

4.2. Conversion Accuracy as a Function of Clock Voltage

Figure 12 confirms that for lower clock voltages, i.e. lower voltage applied to the gate of M_5 during the reset phase, a finer comparison can be made on the input signal. The voltage gain in the p -type differential pair is increased by lowering the clock voltage, so the input offset can be adjusted with higher resolution at the cost of longer reset time and longer overall adaptation. If the clock voltage is too low ($<2.1 \text{ V}$), reset will be incomplete, resulting in hysteresis in the comparison outcome and adaptation. We can avoid this problem by keeping the clock voltage above a value defined by the nFET threshold. Experimentally we find that $742 \mu\text{V}$ is a lower-limit for the input-referred noise σ_n . This exceeds the standard deviation of the input-referred offset (post adaptation) $\sigma_n > \sigma_o$, which confirms that the input-referred noise dominates resolution. Assuming that the input signal has a 3.3 V peak-to-peak swing, $\sigma_n = 742 \mu\text{V}$ translates into 63.9 dB SNR or equivalently, 10 effective bits in a single comparison. By averaging over several adaptation cycles we can reduce the contribution of circuit noise to reach the limiting resolution provided by the offset adaptation procedure ($\sigma_o = 379 \mu\text{V}$), which translates into 78.8 dB SNR

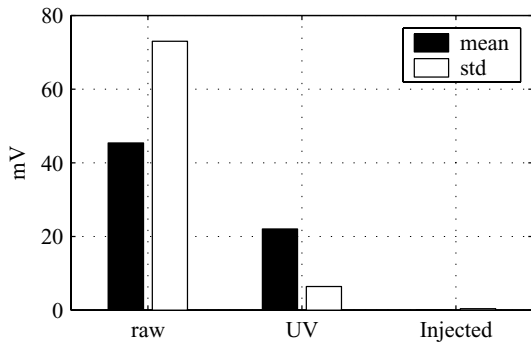


Fig. 11. Mean and standard deviation of input-referred offset measured before adaptation (left), after UV erasure (middle), and after adaptation (right).

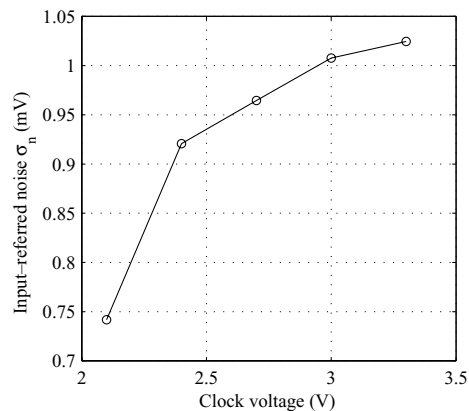


Fig. 12. Conversion accuracy depends on the clock voltage V_{clk} . Accuracy increases with circuit gain as V_{clk} is reduced.

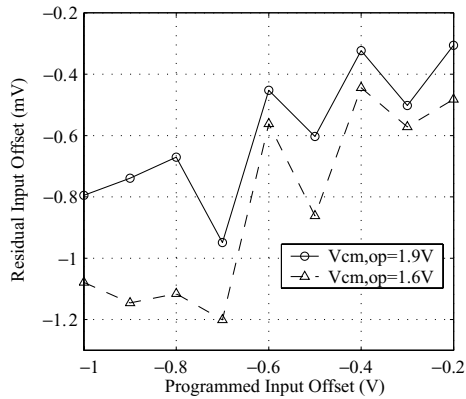


Fig. 13. Residual input offset voltages remain small over a wide range of programmed offset voltages.

or 13 effective bits. In this experiment, we used a bias current of $40 \mu\text{A}$, V_{CM} of 1.2 V, V_{dd} of 4 V, and $V_{\text{dd}2}$ of 3.3 V, corresponding to a power consumption of $160 \mu\text{W}$.

4.3. Input-Referred Offsets Programmed Over ± 1 V Range

The AFGC can automatically cancel input offset, as shown above, or can be used to program a desired offset over a wide range of input values. Figure 13 shows the residual input offset voltages after programming different offsets ranging from -1 V to $+1$ V. These experiments used $V_{\text{CM}} = 2.5$ V for injection. The voltage residue is defined to be the measured input offset minus the programmed input offset. The solid trace shows the input offsets measured for $V_{\text{CM}} = 1.9$ V, and the dashed trace shows the result when measured for $V_{\text{CM}} = 1.6$ V. Larger shifts of V_{CM} from injection conditions result in larger offset errors during operation. This is caused by Early voltage mismatches on the p -type differential pair and channel length modulation on the pFET that provides I_{bias} for the p -type differential pair.

4.4. Time Course of Offset Adaptation

Figure 14 shows the time course of adaptation. We first introduce a 0.2 V input offset on the gate, and then pulse the V_{CM} to an appropriate injection voltage (between 3 and 3.3 V) for 10 ms (1000 clock cycles) with $V_d = 0$ V and the clock running at a frequency of 100 kHz. We take measurements with $V_{\text{CM}} = 1.9$ V between

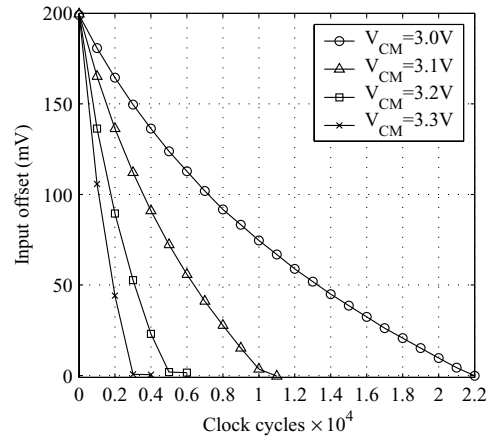


Fig. 14. Input offset decreases exponentially in time. Offset is initially 200 mV and decreases in time, with decay time constant increasing with V_{CM} .

each pulse. We can see that for higher programming V_{CM} we achieve faster convergence. The time course is roughly exponential, as predicted by the injection model in Eq. (1). After the offset reaches 0 V it remains there, for all values of V_{CM} .

Assuming that the input offset voltage μ decays exponentially with injection time constant τ_j from an initial value $\mu_0 = 200$ mV, the input offset decays as $\mu(t) = \mu_0 e^{-t/\tau_j}$. From the experimental data $\mu(t)$ we can estimate τ_j . The estimates are depicted as ‘+’s in Fig. 15 as a function of V_{CM} . The injection time constant ranges from 100 ms for $V_{\text{CM}} = 3$ V to 18 ms for $V_{\text{CM}} = 3.3$ V. The injection time constant decreases exponentially with V_{CM} , i.e. $\tau_j(V_{\text{CM}}) = \tau_{j0} e^{-k(V_{\text{CM}} - V_{\text{th}j})}$, which is consistent with our simple model of injection. The time constant τ_j is inversely proportional to the injection current, which in turn is roughly exponential in drain to gate voltage. The gate-to-drain voltage scales with V_{CM} , and $V_{\text{th}j}$ is the “injection threshold voltage”. We fit the data in Fig. 15 with a dashed line corresponding to $\tau_{j0} = 1$ s, $k = 6.43$ and $V_{\text{th}j} = 2.64$ V. Experimentally we find injection starting around $V_{\text{CM}} = 2.5$ V with adaptation occurring within seconds, confirming the accuracy of this simple exponential approximation.

4.5. Overshoot

The results described in previous sections have been obtained using the dynamic adaptation method, with a running clock and injection occurring during the

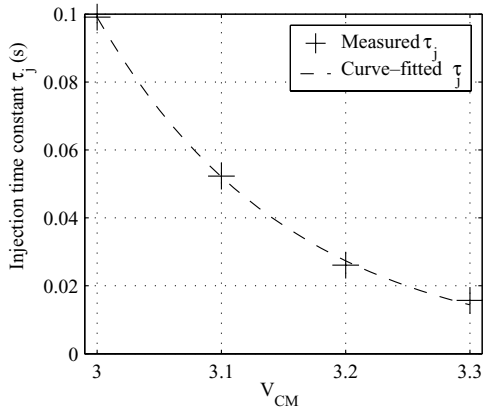


Fig. 15. Measured and inferred injection time constant τ_j vs. V_{CM} .

evaluation phase of operation. If we supply a constant high voltage at the clock terminal as occurs during the reset phase, the comparator becomes an amplifier with gain determined by the clock voltage. We perform static injection on the comparator in this amplifier configuration and observe the injection behavior. Figure 16 shows an injection time course for a constant voltage of 3 V applied to the clock terminal. The setup is similar to the previous experiment (injection time course), but with a higher V_{dd} (5.3 V) and a longer V_{CM} pulse period (100 ms). As before, we program an initial input offset of 0.2 V, and record the input offset once every 0.1s during injection. As depicted in Fig. 16, the input offset voltage does not stop when the offset reaches 0 V at

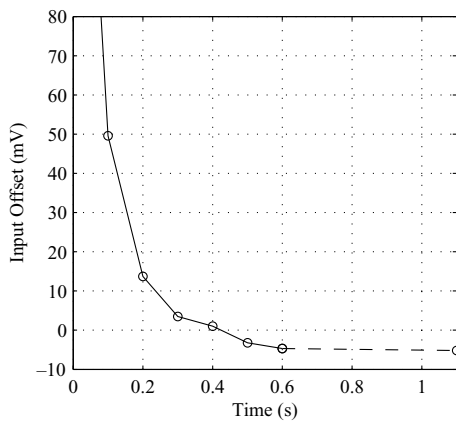


Fig. 16. Input offset for the static injection method with clock held constantly high. Offset first decreases, then “overshoots” the desired point and settles at a nonzero offset voltage.

time 0.4s, but rather continues to drop. This overshoot phenomenon exists because the injection currents become unbalanced during programming. The injection currents are proportional to the channel currents of the p-differential pair, and these currents are changing in value due to the correction. Note that the equilibrium does not imply equal channel currents or equal output voltages, since injection depends on both channel current and gate-drain voltage.

4.6. Temperature Dependence

To verify robustness of the AFGC, we measured the input-referred offset voltage over a 20°C temperature range. The test fixture is placed on a hot plate with simple thermal insulation. A temperature sensor is attached to the top surface of the 40-pin DIP ceramic chip package. The comparator is calibrated with 100 mV input offset at the two extreme temperatures, and input-referred offset error is measured at intermediate temperatures. First, we calibrate the comparator at 27.0°C. The solid trace in Fig. 17 shows the residual input offset measured as the temperature increases up to 50.0°C. Next, we perform adaptation at 50.0°C, and record the residual input offset measures as the temperature decreases down to 29.7°C (dashed trace).

The accuracy of adaptation does not exhibit discernible variation with temperature. When calibrated at temperatures of 27.0 and 50.0°C, the error is

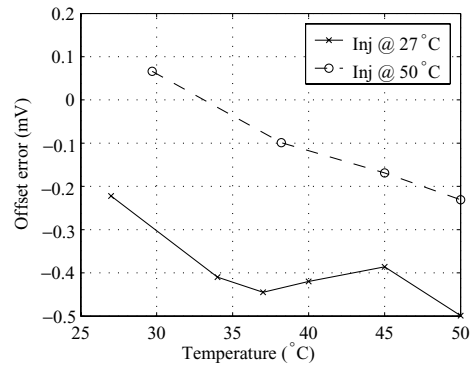


Fig. 17. Input offset voltage error of the AFGC measured over a range of temperatures from room temperature (27°C) to 50°C. Data is shown for a single comparator, first calibrated with an initial offset of 100 mV at room temperature. As the temperature increases the offset error decreases. Subsequently the comparator was calibrated with an initial offset of 100 mV at 50°C. As the temperature decreases from 50°C the offset error increases.

-222 and $-204 \mu\text{V}$, respectively. Once calibrated at a given temperature, however, the input-referred offset does vary with temperature. From the data in Fig. 17, the temperature coefficient is roughly $-15 \mu\text{V}/^\circ\text{C}$. Differential circuits are inherently tolerant to globally applied perturbations, and consequently the temperature drift is more than two orders of magnitude less than $-2.4 \text{ mV}/^\circ\text{C}$, the threshold voltage drift for an ordinary CMOS process [32].

4.7. Offset Charge Retention Time

While most of the measurements reported thus far (Sections 4.1–4.6) have been obtained over relatively short time periods, the ability to program an offset voltage which is retained over an extended period of time is highly desirable. We have confirmed experimentally that the floating gate comparator accurately retains offset for more than a month. Figure 18 shows residual input offset measurements for two different chips, one programmed initially with 0 V input offset, and one programmed initially with 100 mV input offset. In between each measurement, the chips are removed from the test fixture and stored on conductive foam. We perform the measurements using standard ESD protection but no other special precautions.

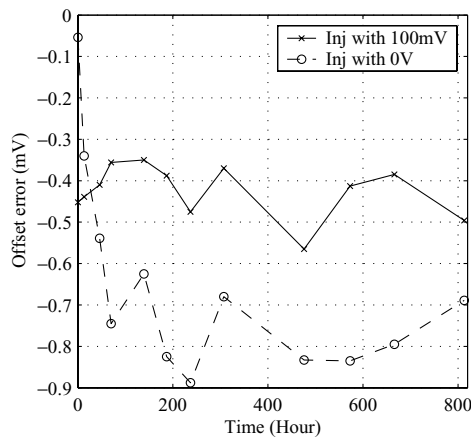


Fig. 18. Residual input offset voltage error of the AFGC measured over a 34-day period. Data is shown for two comparators, calibrated with initial offsets of 0 V and 100 mV respectively. In between each measurement the chips are removed from the test board and stored under ordinary lab conditions. Measurements of the two comparators occurred simultaneously, and systematic variation of the measured offsets is apparent. This variation is likely due to ambient temperature fluctuations.

For the chip programmed with 100 mV, the error stays around $-450 \mu\text{V}$. For the chip programmed with 0 V, the offset drifted by $691 \mu\text{V}$ in the first 3 days, then stayed around $-750 \mu\text{V}$ through the end of the experiment. The initial drift is likely to be due to the relaxation mechanisms or to residual injection with the inputs at the common mode voltage used for evaluation. The drift stops in the fourth day. During the measurement period there is systematic variation observed on both chips; these variations are likely to be caused by ambient temperature fluctuations in the laboratory setting.

5. Conclusion

In this paper we presented the technique of *differential hot electron injection* for adapting and storing signed state variables using floating gates. This approach is compatible with all modern digital CMOS technologies and can be readily extended to novel circuit applications. The method has been previously reported in linear circuit architectures using nonlocal control of the adaptation. In this work we have extended this method for a nonlinear circuit, which provides a highly compact and robust implementation of a comparator. The technique takes advantage of impact-ionized hot electron injection currents, usually considered “undesirable” for submicron circuit design, and uses them to *improve* circuit performance and *reduce* layout area rather than “fight” the physics.

The adaptive floating gate comparator uses pFET hot-electron injection in a negative feedback loop during adaptation and programs nonvolatile corrective charges on the floating gates. The load for the input differential pair is a regenerative element which computes the outcome of the comparison and inherently presents appropriate voltages for *locally* programming the input floating gate nodes. The technique is not limited to local adaptation and we are currently extending it for the case of nonlocal adaptation which allows greater flexibility in design.

Experiments show that adaptation consistently produces residual offset which is a fraction of input-referred noise for all observed values of injection mismatch. We experimentally demonstrate more than two orders of magnitude reduction in offset voltage: the mean offset is reduced by a factor of 416 relative to

fabricated chips directly from the foundry and by a factor of 202 relative to UV-irradiated chips. The adaptation encompasses the entire comparator circuitry and therefore the residual offset is independent of initial device offset. We consider both static and dynamic adaptation and conclude that the accuracy of offset cancellation using the dynamic paradigm is approximately two orders of magnitude better than the static paradigm. In the presence of observed 8% injection mismatch, the AFGC robustly converges to within $728 \mu\text{V}$ of the desired input offset (mean offset $-109 \mu\text{V}$, standard deviation $379 \mu\text{V}$). Offset cancellation is achieved within milliseconds. We report charge retention after adaptation for more than one month, and show that after adaptation the variation of offset error with temperature is $-15 \mu\text{V}/^\circ\text{C}$, significantly less than the temperature coefficient of typical MOS devices.

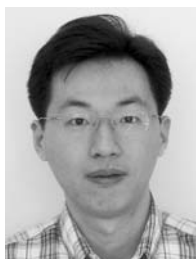
Acknowledgments

We thank the MOSIS service for providing chip fabrication through their Educational Research Program. Y.L. Wong is supported by The Johns Hopkins University Applied Physics Laboratory. P.A. Abshire is supported by an NSF CAREER Award (0238061). The authors thank anonymous reviewers for their insightful comments.

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